Sinusoidal Inverter Using Tap-changer Transformer

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Abstract

This paper presents new technique of multilevel inverter where pulse width modulation technique (PWM) is used, using tap changer transformer. A microcontroller circuit put dc source voltage at the primary tap changing side of transformer by switching, the related switches and eventually controls the volume of the output voltage. On other hand, at the secondary side of transformer, the load is connected. MATLAB model is used to simulate the proposed inverter for thirteen levels. In Proteus/software, Arduino UNO is used for seven levels sinusoidal inverter. Finally, Designed circuit reduced THD of the output voltage grandly.

Keywords: *Multilevel inverter, tap-changer Transformer, Proteus software simulation.*

I. INTODUCTION

Ac power to dc power in power electronics is called ac-dc converter, which used in many applications: power supplies, electric vehicles and dc motor speed control [1, 2]. To convert dc power to ac power an inverter is needed with a suitable output voltage and frequency. High switching losses, less efficiency and high cost , these defects of inverter made orientation to multilevel inverter compare to the conventional bipolar the multilevel inverter output voltage to reduce harmonics [3]. To control the poverty power electronics switches and applications that wanted high current and high voltage the multilevel fundamental switching project is used [4 ,5] . The output achieves near sinusoidal shape, reducing the harmonic as the number of levels increased [6]. In pulse widthmodulation technique (PWM), the amplitude of pulses differs proportionately with the amplitude of analogical useful signal while the width and position of pulses are constant. In PWM, a pulse differs proportionately with the amplitude of analogical useful signal while position of pulses is constant [7].

In this paper dc – ac converter is worked by using tap changing transformer. Two dc sources are connected on the terminals of switches. To make output voltage sinusoidal these switches deference the primary turns of the transformer where these switches pass dc source on the primary side of tap changer transformer. A controller circuit, controls power switchingsuch a way to shape vary the magnitude of output voltage. At the secondary side of the tap changer transformer the load is connected when upper switches are switched at sequence method the positive half cycle consist.Similarly, at switched lower, switches of negative half cycle is connected. THD is reduced by using this technique.

II. TAB-CHANGER INVERTER

Figure 1 shows the proposed inverter which is consists of two dc sources as input source, switches (power semiconductor switches IGBT, MOSFET), filter, tap changer transformer and load.

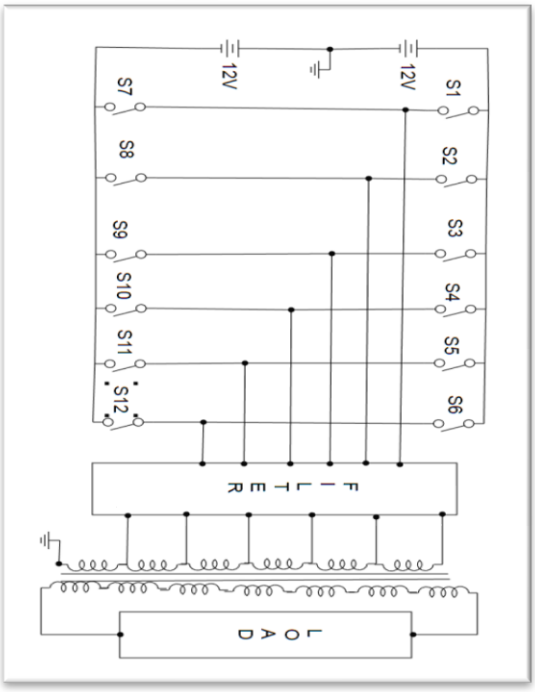

Fig. 1:Proposed circuit diagram of tap changer inverter.

III. OPERATING PRINCIPLE

A- Upper Switches:

Pulse generator given the switches S_1 get to S_6 gate pulses to shape positive half cycle. At the secondary side of transformer output voltage appearing. At operate S_1 get minimum output voltage because S_1 put dc source at the maximum primary turns of the transformer which is given by:

$$V_2 = V_1 \frac{N_2}{N_1} \qquad (1)$$

whereV_1 is the input voltage and V_2 is the output voltage.

In the same way when S_2 switching the output voltage increase where primary turns of transformer decrease. This sequence of increasing output voltage opposite decreasing the primary turns of transformer continue up to switching S_6. Output voltage get maximum value as minimum primary turns of transformer was connected.

B- Lower Switches:

Pulse generator given the switches S_7 get to S_{12} gate pulses to shape negative half cycle. At the secondary side of transformer output voltage appearing. At operate S_7 get minimum output voltage because S_7 put dc source at the maximum primary turns of the transformer. In the same way when S_8 switching the output voltage increase where primary turns of transformer decrease. This sequence of increasing output voltage opposite decreasing the primary turns of transformer continue up to switching S_{12}. Output voltage get maximum value as minimum primary turns of transformer was connected.

IV. MATLAB/SIMULINKMODEL

Tap changer inverter is modeled and simulated using Matlab/Simulink as a tap-changing transformer as shown in Fig.2. IGBT represented the power switches and Pulse generator represented a controller circuit which is used to control the power switches IGBTs.

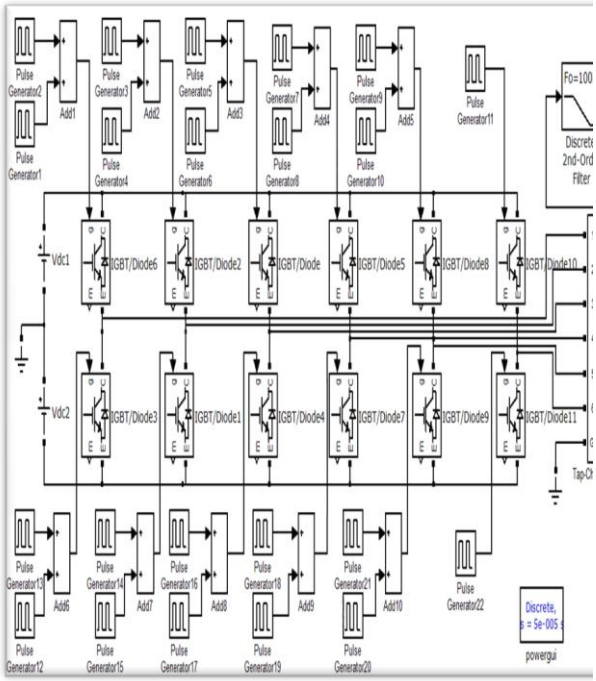

Fig.2: Matlab model thirteen level tab-changer inverter

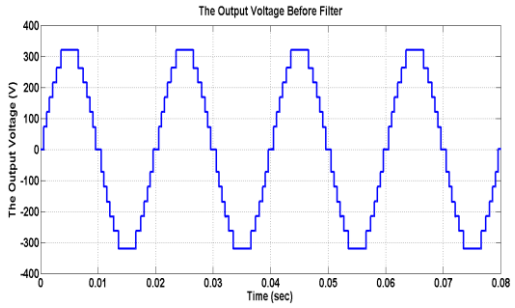

Fig. 3: Output voltage before filter.

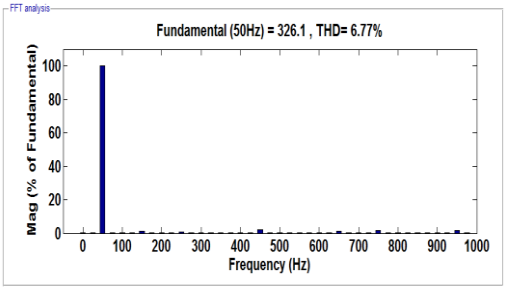

Fig. 4:FFT analysis before filter

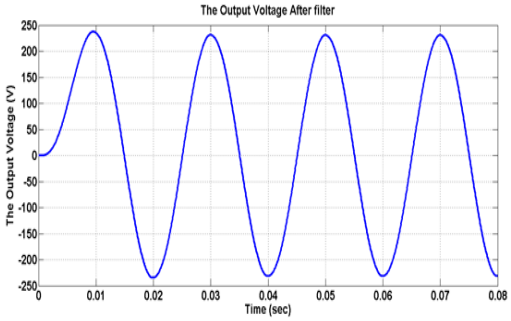

Fig.5: Output voltage after filter

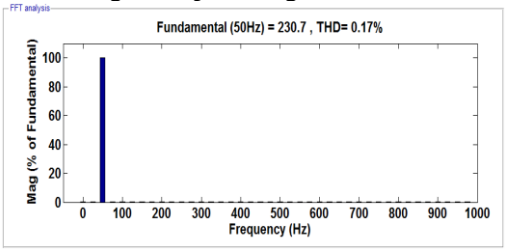

Fig.6: FFT analysis after filter

V. MATLAB SIMULATION RESULTS

Theoutput voltage of the suggested thirteen level inverters is nearing sinusoidal shape before filter and THD is (6.77%) as shown in Fig. (3 and 4) the output voltage exactly sinusoidal and THD is (0.17 %). For this reason, the output voltage in proposed inverter is near sinusoidal shape with little content of THD.

VI. PROTEUS SOFFTWARE

In proteus program tap changer inverter is presented as a tap changertransformer. BDX54 and BDX53 represented the switches with2N222 asdrivers. Arduino UNO represented microcontroller circuit, dc-ac designed circuit shows in Fig. 7.

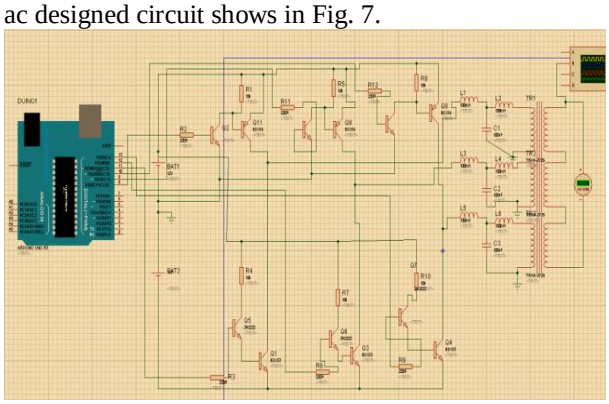

Fig.7: The models of design for seven levels dc-ac inverter.

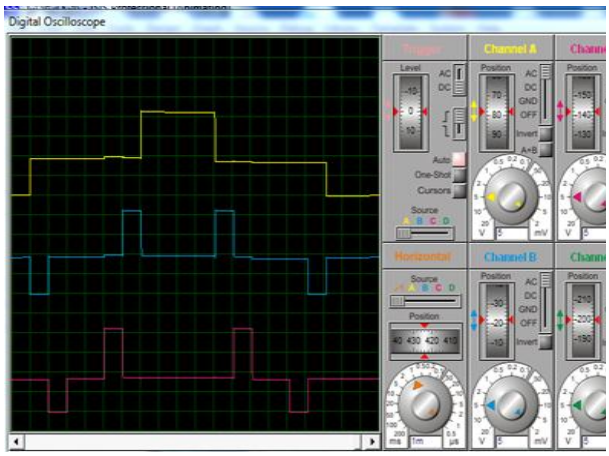

Fig. 8: Output pulses from upper and lower switches without rest.

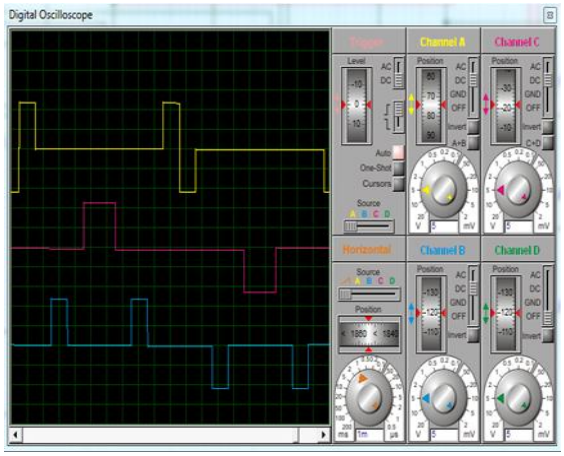

Fig. 9: Output pulses from upper and lower switches with rest.

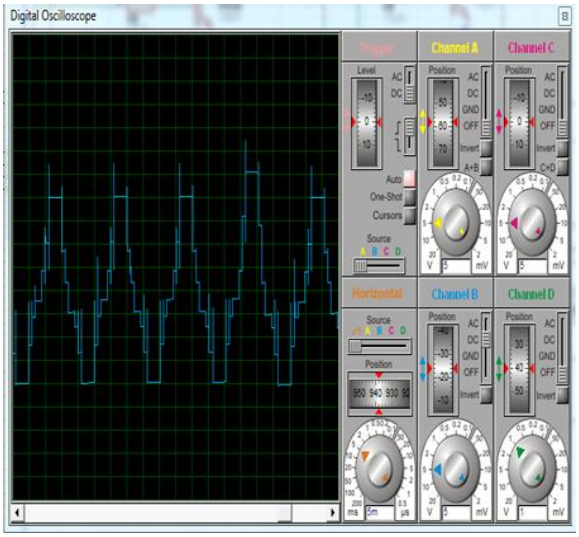

Fig. 10: Output voltage without rest.

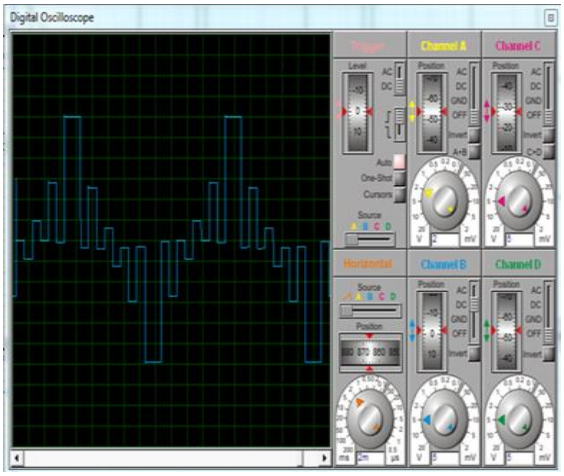

Fig.11: Output voltage with rest.

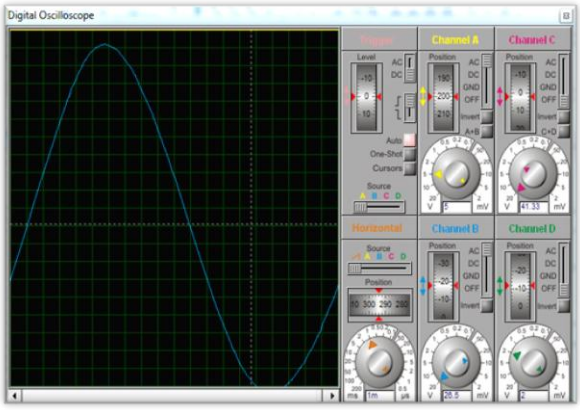

Fig.12: Output voltage after filter.

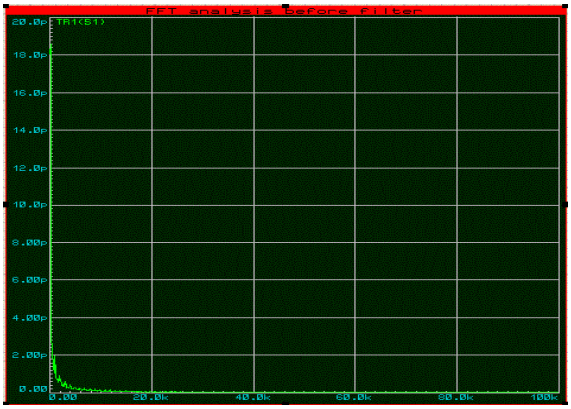

Fig. 13: FFT analysis before filter.

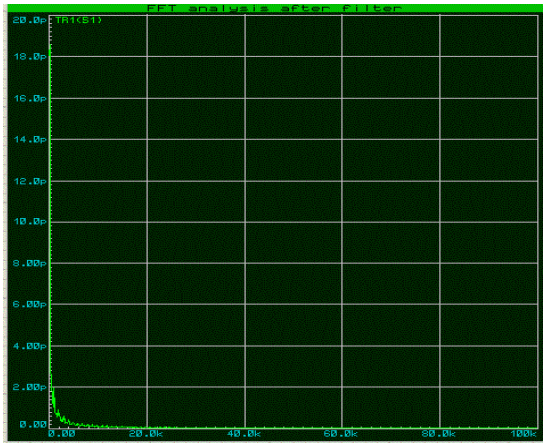

Fig.14: FFT analysis after filter.

VII. CONCLUSIONS

Tap changer inverter is represented by putting dc source to tap changer transformer with the help of the controller circuit during some switches of power semiconductors (IGBT, MOSFET) in chaining modality. THD has been reduced grandly. The increasing of levels leads to decreasing in THD and the output voltage will be more sinusoidal.

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