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*Original Article*

# On-Chip Programmable Ultra-Low Power Fast Data Converter with ALU-based Encoder using Memristor for AI Applications

Md Noorullah Khan[1], E Srinivas[2]

[1,2]*Department of Electronics and Communication, School of Engineering, Anurag University, Telangana, India.*

[1]*Corresponding Author : noorullah.khan@mjcollege.ac.in*

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***Abstract*** *- This paper describes a very high energy efficient Fast Data converter such as flash ADC which meets the requirement for Artificial Intelligence Networks using Memristor, aiming the reprogramming feature it can also be used in Machine Learning, In order to have significant features related to power consumption and area occupied, efficiency as well as conventional CMOS technology compatibility, Memristor is the most suitable circuit component for the applications which require ultra low power consumption, also its non volatile nature makes it to store the data as well with out the need of additional memory circuitry which reduces the chip area as well as power consumption, using this approach a super fast 3-bit ADC such as Flash is designed and simulated in Cadence virtuoso design environment using VTEAM model of Memristor, also the working of the ADC is validated by giving an analog signal producing an accurate digital output signal, with a power supply of 1 volts, the 3 bit ultra low power super Fast ADC has a power consumption of 1.23 mw operating at a speed of 53.19 MHz (18.8 ηs delay). Hence, with this novel architecture using Memristor, the number of transistors is reduced, accomplishing low power and a smaller size.*

***Keywords*** *- Flash ADC, Logic Circuit, Memristor, Opamp, VTEAM.*

## 1. Introduction

The Memristor concept was first proposed by Chua in 1971 [1] as a "missing circuit element",

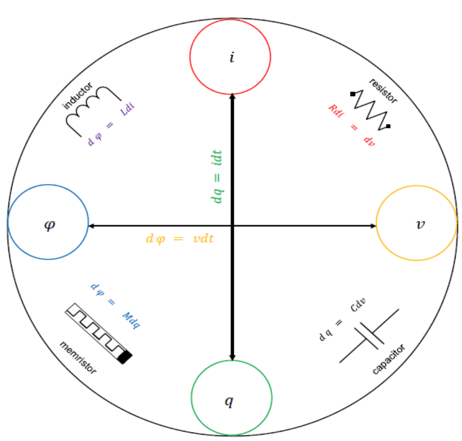



**Fig. 1 Memristor relations with other elements**

The inter-relational ships among the various parameters, such as Voltage, Current (V-I), and Flux, Charge (Ø-Q), as shown in Figure 1, have made the prediction of the 4th fundamental circuit component, called the Memristor. ( memory-resistor ) In addition to the capacitor, inductor, and resistor, in 2008, nearly 4 decades ago, it was confirmed experimentally when Williams, Strukov, and Snider of HP-Labs physically realized the Memristor with Titanium Dioxide (TiO2) using Platinum (Pt) Electrodes [2].

In order to validate Moore's law [3], the device dimensions of the existing CMOS technology scales down which makes it prone to various limitations such as short channel effects, Memristor is an alternative approach which can remove these limitations [4], also the draw backs of Von Neuman architecture which has separate storage and processing units can be overcome by using memristors as a promising solution which makes it to achieve "In - memory computation" which drastically increases the computation speed required by the modern artificial intelligence devices also by reducing the size and power used, also memristors are compatible with CMOS technology where they can be used in metal layers [5], programming of the Memristors can be performed by applying a bias voltage [7] and even if the power supply is removed [8] they can retain their state for which it can be used as (NV-RAM) Nonvolatile Random Access Memory [9], Artificial Neural Networks can be realized using memristors [10] where they can be programmed as a neuron comprising of synapse, Axon, Dendrites as shown in Figure 2, for Artificial Intelligence applications where the Memristor can be used to reprogramme the bias voltage [11], also digital logic circuits can be made functional with Memristor based logic in order to have low power [12], chaotic circuits [13] which is a non-periodic oscillator [14] producing waveforms used in sound generation and random signal generation used in Cryptography [15]. A brief overview and potential applications, such as memory, storage, and “in-memory computation,” are discussed in [16].

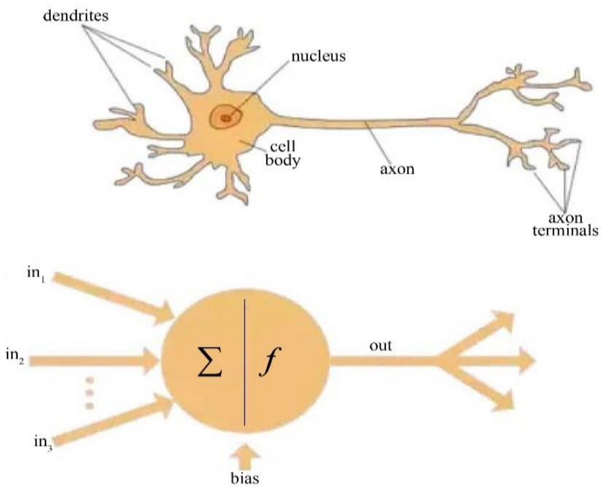



**Fig. 2 Memristor relations with other elements**

However, the most significant challenge faced by te Flash ADC is the amount of hardware required, particularly the number of comparators, which drastically increases the chip area.

For high-resolution circuits, the circuit size increases exponentially, since for “n” bits of resolution, the number of comparators required is $(2^n – 1)$, which ultimately consumes high power. Hence, innovative ADC designs are required with new components such as memristors, for which the traditional CMOS technology is not feasible for AI applications.

In order to over-come the potential limitations on power, area and speed, memristors are used in designing of the flash ADC along with the digital logic, The organization of the paper is outlined in the following sections, in Section 2 memristor architecture and their relations are discussed, Section 3 discusses the design of different digital logic circuit, for which it can be interfaced with CMOS transistors and sequential circuits, Section 4 integrates all the blocks to the overall flash ADC architecture, and lastly Section 5 deals with conclusion.

### *1.1. Memristor Architecture*

The voltage and current mathematical relations of the Memristor are given by:

$$V(t)=M\,(q(t))*i(t) \tag{1}$$

Where M represents the memristance and i, v, and q represent current, voltage, and charge, respectively, Also, the flux and the charge with memristance are interrelated as shown,

$$d(\emptyset) = M\,d(q) \tag{2}$$

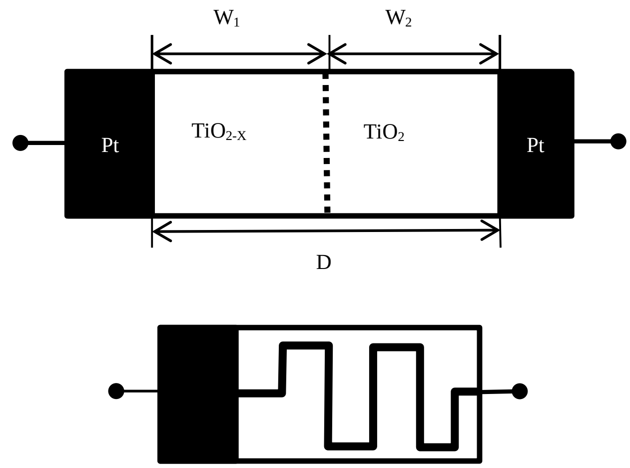



**Fig. 3 Memristor architecture structure and symbol**

The memristor architecture is as shown in the above Figure 3 where it is build by taking the material Titanium Dioxide ($TiO_{2-X}$) Doped (deficient of oxygen atoms) hence positively charged and Un-Doped ($TiO_2$) with Platinum (Pt) electrodes on either side, the doped and undoped regions widths are represented by $W_1$ and $W_2$ respectively, the combination of the widths of these regions gives rise to the total width which can be given as $D = W_1 + W_2$. With the application of a forward bias voltage, the doped region ($TiO_{2-X}$), which has positively charged oxygen ions, gets repelled and will be diffused into the Undoped Region ($TiO_2$) by reducing the resistance to a low value given by $R_{ON}$, which results in the flow of current [27].

Conversely, applying a reverse bias voltage will reverse the action by making the ions in the Undoped Region ($TiO_2$) drift towards the previously Doped Region ($TiO_{2-X}$), which increases the resistance, resulting in ($R_{OFF}$) indicating high resistance. The electrical symbol of the Memristor is shown in Figure 3. To simulate the above component, a Spice model is prepared as per the given functionality with the equations as represented below[28]. The differentiation relationship of the state variable is given by the following.

$$\frac{dw(t)}{dt} = \begin{cases} K_{OFF}\left(\frac{V(t)}{V_{OFF}} - 1\right)^{\alpha_{OFF}} f_{OFF}(W), & 0 < V_{OFF} < V \\ 0, & V_{ON} < V < V_{OFF} \\ K_{ON}\left(\frac{V(t)}{V_{ON}} - 1\right)^{\alpha_{ON}} f_{ON}(W), & V < V_{ON} < 0 \end{cases} \tag{3}$$

The window functions " $f_{off}(w)$ " and " $f_{on}(w)$ " are used to limit the value of "w" between 0 and 1. $k_{on}$, $k_{off}$, and $\alpha_{off}$, $\alpha_{on}$, are fitting parameters, and the threshold voltages are represented as $V_{on}$ and $V_{off}$. Also, for the VTEAM model [32], the current voltage relation is governed by:

$$i(t) = \left[R_{ON} + \frac{R_{OFF}-R_{ON}}{W_{OFF}-W_{ON}}(W - W_{ON})\right]^{-1} V(t) \quad (4)$$

Where "$W_{ON}$" and "$W_{OFF}$" represent the boundaries of "w" (state variable), the ON & OFF resistances are represented by "$R_{ON}$" and "$R_{OFF}$" respectively,

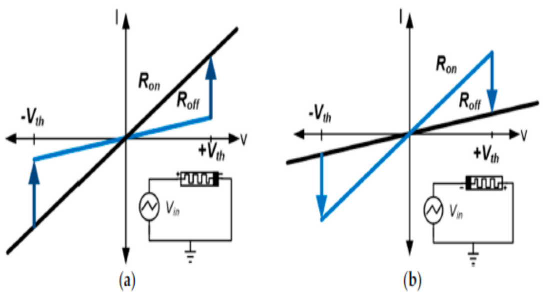



**Fig. 4 V-I Characteristics of memristor**

The above Figure 4 shows the V-I characteristics, which indicate the pinched hysteresis at the origin for the simulations performed for the above memristor models.

## 2. Operational Amplifier

### *2.1. Conventional Operational Amplifier*

The traditional Opamp represented in Figure 5 uses a fixed resistor as a load, which is not suitable for present AI-based applications where the reprogramming feature is essential.

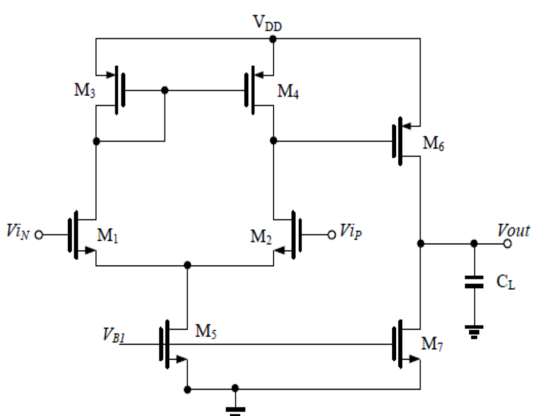



**Fig. 5 Operational amplifier circuit schematic**

The opamp forms the fundamental block of the ADC architecture, comprising two stages. The differential gain stage forms the input stage. The difference between the two input signals is amplified by 1st stage, which helps to combat the noise signals at the input itself. In order to obtain high gain, the first stage output is given to a common source amplifier comprising the 2nd stage.

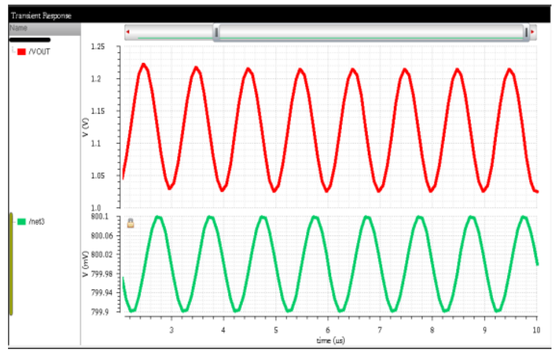



**Fig. 6 Opamp transient simulation results for a sine input**

The opamp output results show that for an input signal of 800 mV, the output has been significantly amplified to a 1-volt range, as shown in Figure 6.

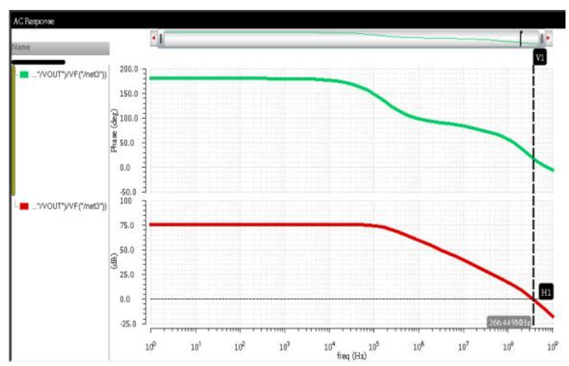



**Fig. 7 Gain and the phase plot of the operational amplifier**

The gain and phase plot of an opamp with a fixed load is shown above in Figure 7.

### *2.2. Novel Operational Amplifier with Memristor Load*

With the emerging component, such as Memristor, which has a reprogrammable feature, the resistance can be varied for a wide range, which can be suitable for Artificial-Intelligence (AI) based applications, as shown in Figure 8.

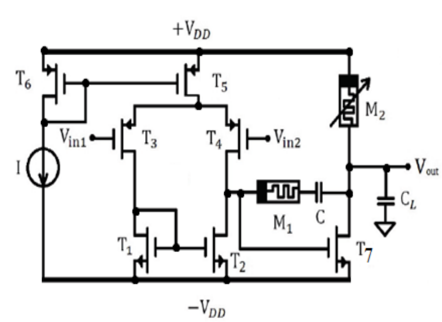



**Fig. 8 Operational amplifier with a programmable memristor**

The gain of an opamp with a memristive load can be written as:

$$A = \frac{g_m R_l}{1 + j\,\omega\, R_L\, C_L} \qquad (5)$$

Where "$g_m$" is the transconductance of the input transistor, "$R_m$" is the mem-resistance, and "$C_L$" is the load capacitance.

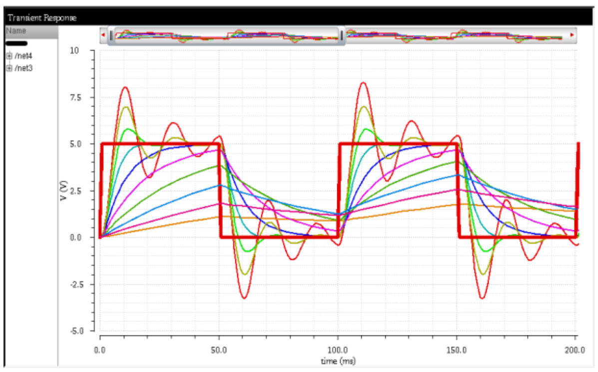



**Fig. 9 Square input response of the operational amplifier with a programmable memristor for different values of resistance**

As the load resistance (Mem-resistance) is varied, we get different waveforms as shown in the above Figure 9 for a square wave input,

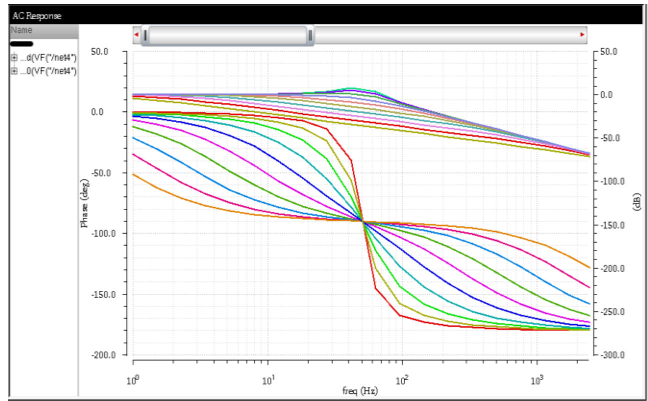
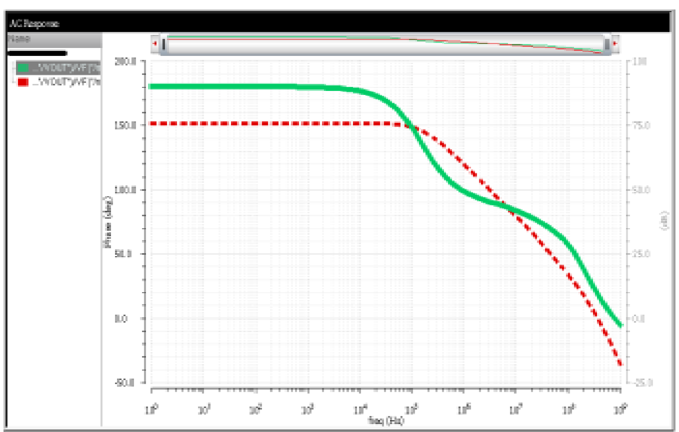
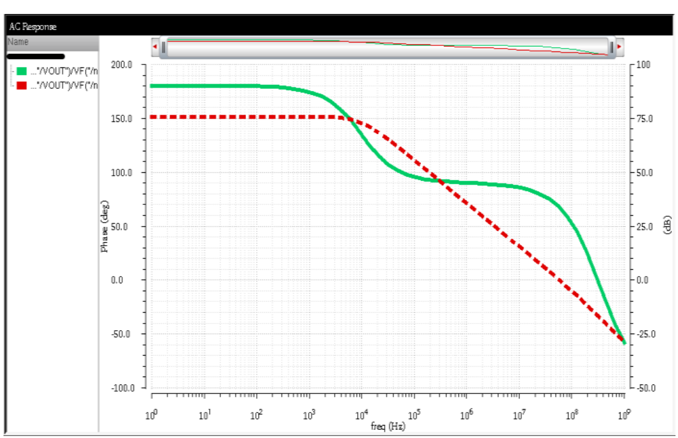



**Fig. 10 Opamp gain-phase plot with variable memresistance**

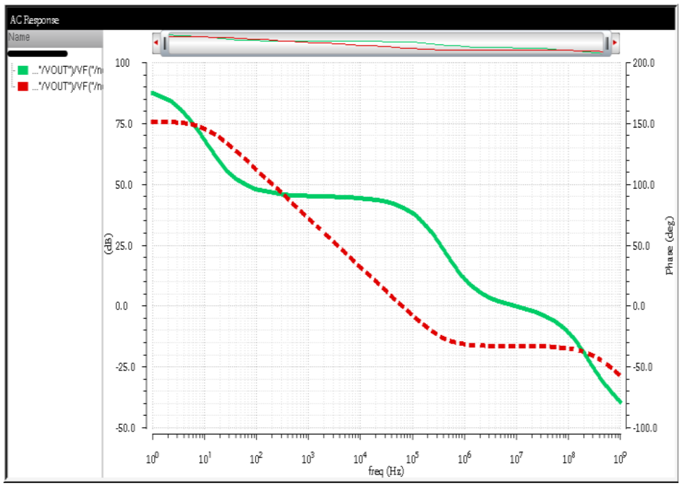
Also, the gain and the phase plot for different mem-resistance is shown as above, in Figure 10. Also, with the variation in the load resistance and the load capacitance, we get different gain and phase plots as shown in the above Figure 11.



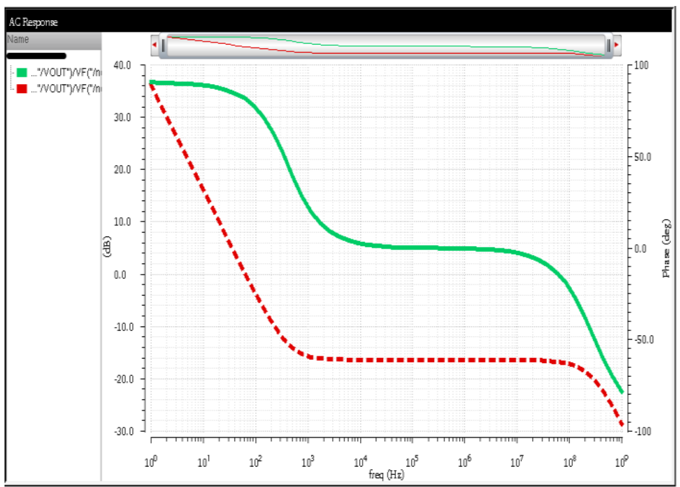

**(a)**




**(b)**




(c)




(d)

**Fig. 11 Gain-phase plot of Opamp with variable memresistance**

## 3. Logic Gates using Memristor

Logic gates can be implemented using memristors, which can have great potential to replace CMOS, as the number of transistors required is doubled to implement in CMOS when compared with memristors, which typically require Half of the quantity. Different logic styles are available to design the Memristor-based circuits; the first two techniques are Imply [30] and MAGIC [31], which are complex and time-consuming due to sequential operation, and the third is the MRL [3] technique, which is going to be implemented over here due to its simplicity and compatibility with the CMOS.

The different digital logic gates building blocks using memristors using the MRL technique are given as shown in the next section.

### *3.1. Memristor-based and NAND Logic Gate*

For the above circuit of AND, the operation is as follows, when ever the input –A and the input-B are given as logic “1” or as logic “0” i.e for ( AB = 00, AB = 11), there exist no flow in current from input to out put since there is no potential difference, hence the output is same as the input applied [3, 29-31],

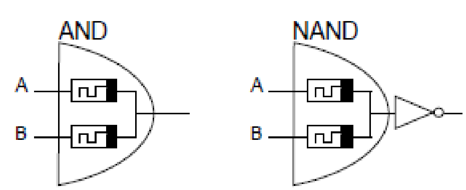



**Fig. 12 Memristor-based AND-NAND logic gate.**

**Table 1. Functionality of AND, NAND Gate, and LOGIC gates**

| a | b | AND (output) | NAND (output) |
|---|---|---|---|
| 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 |

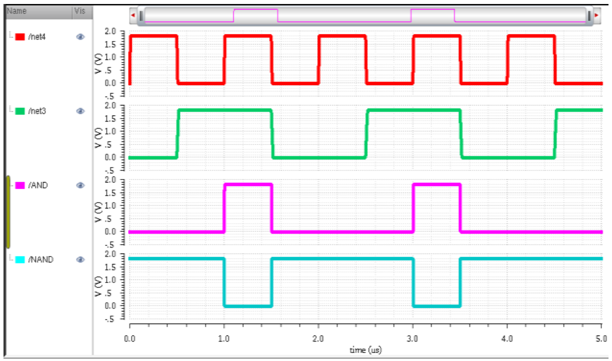



**Fig. 13 Simulated output results of memristor-based AND-NAND logic gate**

Hence, from the above table, the output is logic 0 (low) for the inputs (AB = 00, Low-Low), and the output is logic 1 (high) for the inputs (AB = 11, High-High)

$$V_{out,AND} = \left(\frac{R_{ON}}{R_{ON}+R_{OFF}}\right) V_{CC} \approx 0 \qquad (6)$$

However, whenever the input is either logic-0 or logic-1, for logic-0 as the input the Memristor gets turned "OFF" (high resistance state) and the output gets connected to logic-0 through the Memristor which is "ON" (low resistance state), hence for the AND gate the output remains at low value given by equation (6), also the functionality is indicated in Table 1.

### 3.2. Memristor-based OR-NOR Logic Gate

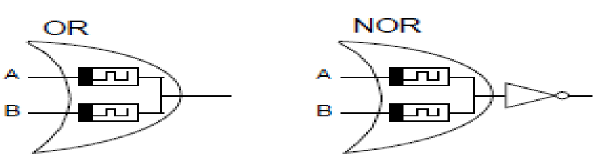



**Fig. 14 Memristor-based OR-NOR logic gate.**

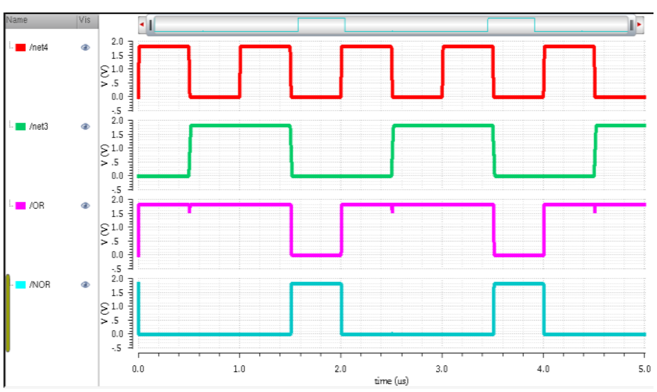



**Fig. 15 Memristor-based OR-NOR Logic Gate Simulation Results.**

For the above circuit of OR gate the operation is as follows, whenever both the inputs are at logic-1 or at logic-0 i.e for ( AB = 00, AB = 11), there exist no flow in current from input to out put since there is no potential difference, hence the output is same as the input applied [29-31,

$$V_{out,OR} = \left(\frac{R_{OFF}}{R_{ON}+R_{OFF}}\right) V_{CC} \approx V_{CC} \qquad (7)$$

**Table 2. Functionality of OR, NOR gates**

| a | b | Out-OR | Out-NOR |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

However, when the input is either logic 0 or logic 1, for the "OR" gate, which is "ON", the output remains a high value given by equation (7), and the functionality is expressed in Table 2.

## 4. Design of the Flash ADC

### 4.1. Conventional Flash ADC with Resistor Ladder Network

The block diagram of a conventional flash ADC is depicted in the Figure 16, where it consists of a resistor Ladder network to generate a reference voltage which acts as a reference for the power hungry comparators, The input analog signal is evaluated against the reference levels generated by the resistor ladder, based on which the comparator produces a decision and gives the output as logic-0 or logic-1, the output of these comparators are then converted to a meaningful binary format by using an encoder such as a Full adder based approach which results in less power consumption, The number of comparators used is given by equation 6,

$$\text{No of Comparators} = (2^n - 1), \qquad (8)$$

where "n" represents the number of bits.

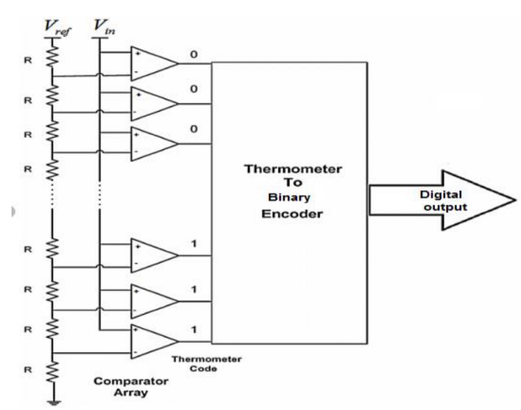



**Fig. 16 Conventional Flash ADC Block Diagram.**

### 4.2. Novel ALU-based 3-Bit Flash ADC using Memristor

Arithmetic and Logic Unit (ALU) can be realized by using a Full adder block, which is comprised of 2 half adder modules along with an additional extra gate, such as "OR."

*4.2.1. Half Adder*

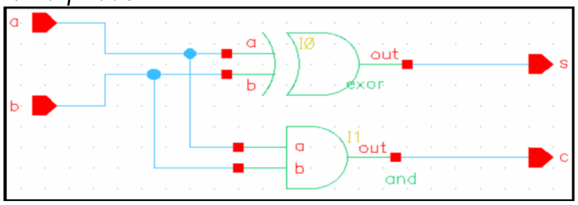



**Fig. 17 Memristor-based Half Adder Block.**

A half adder can be implemented by using an Exor gate and an AND gate, as shown.

The equation of the sum and the carry is given as:

$$S = a \oplus b \tag{9}$$

$$C = a.b \tag{10}$$

*4.2.2. Full Adder*

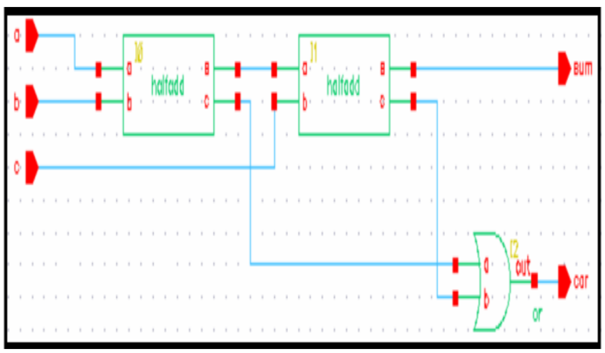



**Fig. 18 Full Adder Implementation Using Memristor**

$$S = a \oplus b \oplus c \tag{11}$$

$$C = a.b + (a \oplus b).c \tag{12}$$

$$C = a.b + b.c + c.a \tag{13}$$

For a full adder, which can be implemented with 2 half adders and one additional OR gate, the sum and carry relations are as shown above in equations (11) and (12).

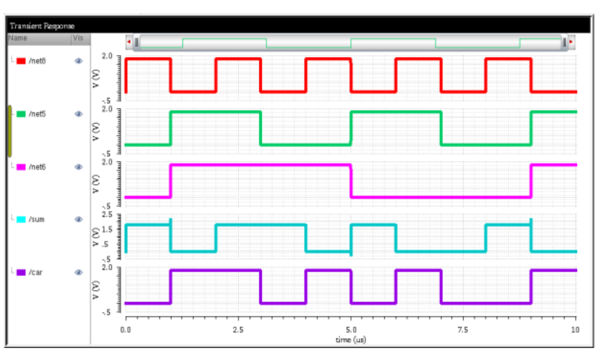


**Fig. 19 Simulated output results of memristor-based full adder block**

*4.2.3. ALU-based Encoder*

ALU as an encoder is required to convert the output of comparators to a meaningful binary pattern, The Arithmetic and Logic Unit consists of adder blocks, which act as ALU since they can perform Logical AND, OR, EXOR, Inversion operation, “Adder” block is called as ALU, hence with the help of this ALU the outputs of the comparators are added in a particular fashion as shown in Figure 20 resulting in a understandable binary code format, The outputs of the Encoder are verified in the simulation results, as shown in Figure 21.

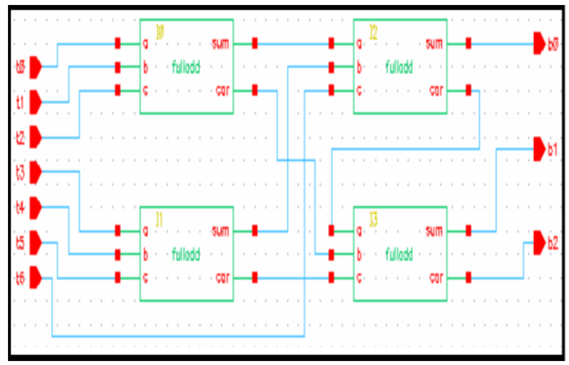



**Fig. 20 Block diagram of alu-based encoder**

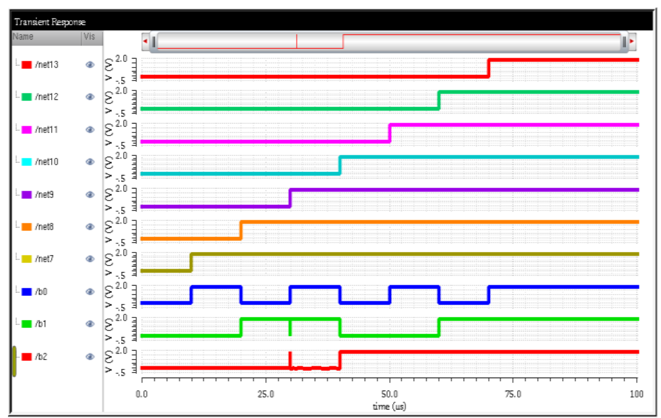


**Fig. 21 Encoder output showing the thermometer code**

In this case a full adder is used as an encoder which adds the number of bits of the thermometer code and convert it to its respective binary code, Table 3 describes how the code conversion process occurs with the application of increasing input voltage signal, the corresponding comparators which exceeds the threshold reference voltage gets triggered by making the output as high “Logic 1”, if we read the above table from right to left in any row of the comparator outputs we find like a thermometer code with increase in mercury level.

Also, a full adder is a core component of a processor as it performs different ALU operations, hence it is also called an ALU, which is used in a processor. Hence, in this design, a processor-based Encoder is used, which is faster than a normal encoder.

**Table 3. Analog input to digital output code conversion process**

| Analog input | Outputs of 7- Comparators | | | | | | | 3-bit Digital output | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_i$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | $d_2$ | $d_1$ | $d_0$ |
| $0 < V_I < \frac{V_R}{8}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $\frac{V_R}{8} < V_I < \frac{2\,V_R}{8}$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| $\frac{2\,V_R}{8} < V_I < \frac{3\,V_R}{8}$ | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| $\frac{3\,V_R}{8} < V_I < \frac{4\,V_R}{8}$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| $\frac{4\,V_R}{8} < V_I < \frac{5\,V_R}{8}$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| $\frac{5\,V_R}{8} < V_I < \frac{6\,V_R}{8}$ | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| $\frac{6\,V_R}{8} < V_I < \frac{7\,V_R}{8}$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| $\frac{7\,V_R}{8} < V_I < V_R$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Hence the code converter is also called as Thermometer to binary Encoder, also the priority encoder can be implemented using adder where the addition of the thermometer bits give rise to the same value as it can be verifier from the truth table The simulations are carried out in Cadence Virtuoso design Environment using VTEAM model [32] and the results are as shown in Figure 21, Hence by using Memristor based approach, we can achieve very low power consumption, the schematic is represented as shown in Figure 20.

*4.2.4. Flash ADC Final Circuit*

From the above waveform, it can be seen that when the input analog signal is high, the digital outputs are logic 1, and when the input is low, the binary outputs become logic zero.

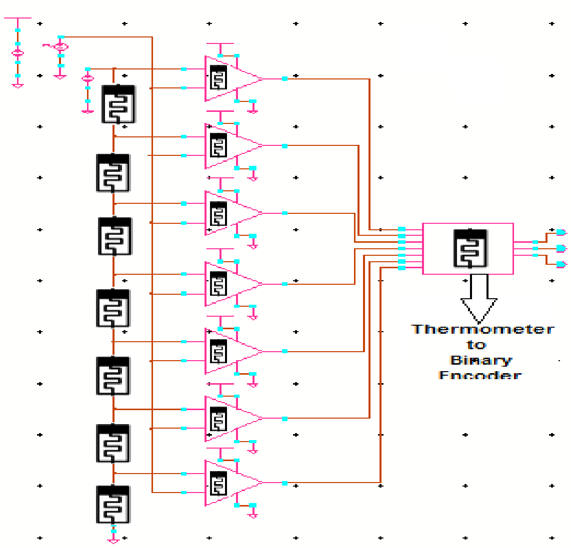



**Fig. 22 Novel memristor-based flash ADC block schematic**

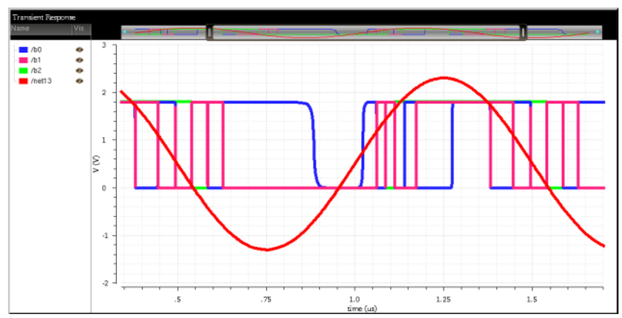


**Fig. 23 Simulation Results of Flash ADC with Overlapped Bits**

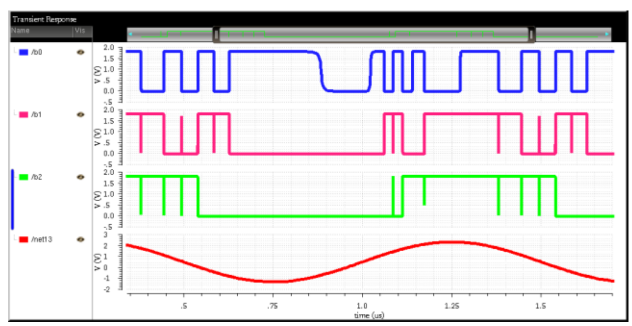


**Fig. 24 Simulated output of 3-bit flash ADC non-overlapped bits**

With the non-overlapping wave forms of the output code of the flash ADC, it can be seen very clearly that when the input signal gets increased, the magnitude of the Flash ADC digital output gets increased from "000" to "111" as shown in Figure 24. Also, by using the Cadence Virtuoso simulator, the average power was found to be 1.23 mW.

A Monte Carlo–based statistical analysis is performed to assess the robustness of the proposed flash ADC design under variations in passive component values, including Process, Voltage, and Temperature (PVT) fluctuations, as shown in Figure 25.

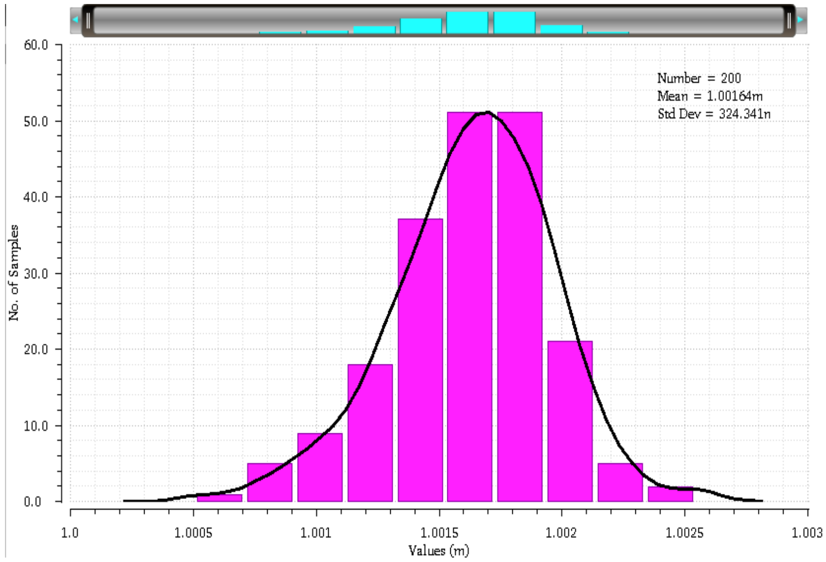



**Fig. 25 Monte-carlo simulated output of 3-bit flash ADC bits**

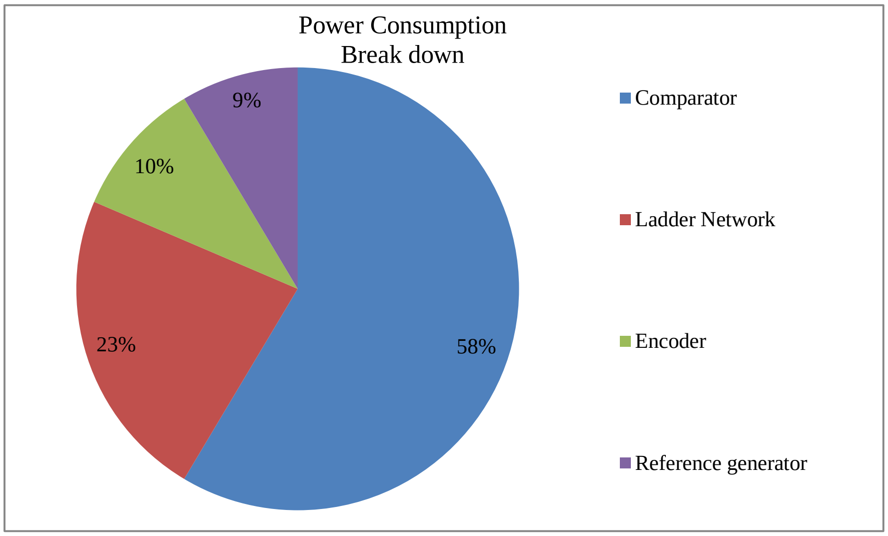



**Fig. 26 Power breakdown of 3-bit flash ADC bits**

The total power consumed by various modules in the Flash ADC is depicted as shown in the above graph, for which we can see that the comparator block comprising an opamp results in more power consumption when compared with the other blocks.

For a conventional N-bit flash ADC, the number of comparators required is expressed as:

$$N_C = 2^N - 1 \tag{14}$$

The total power consumption is approximately:

$$P_{TOTAL} = P_{REF} + N_C \,.\, P_{COMP} + P_{DIGITAL} \tag{15}$$

where $P_{REF}$ is the reference-generation power (typically from a resistor ladder), $P_{COMP}$ is the power per comparator, and $P_{DIGITAL}$ represents the ALU encoder and logic power.

For a CMOS resistor ladder:

$$P_{REF} = \frac{V_{REF}^2}{R_{LADDER}} \tag{16}$$

In the proposed memristor-based Flash ADC, the nonvolatile memristor references reduce $P_{REF}$ significantly,

$$P_{REF}^{MEMRISTOR} \ll P_{REF}^{CMOS} \tag{17}$$

Hence,

$$P_{TOTAL} \approx N_C \,.\, P_{COMP} \tag{18}$$

**Table 4. Comparison table of related work**

| Type | Ref. [26] | Ref. [25] | Ref. [24] | Ref. [23] | This work |
|---|---|---|---|---|---|
| Voltage (V) | 0.8 | 1 | 1.8 | 1 | 1 |
| Resolution (bits) | 4 | 4 | 4 | 4 | 3 |
| Input signal (V) | 0 to 0.8 | 0.1 to 1 | 0.1 to 1 | 0.6 to 0.9 | 0 to 1 |
| Power (mw) | 118.24 | 0.75 | 7.846 | 15.5 | 1.23 |
| Delay (ηs) | 0.16 | 11 | 100 | - | 18.8 |
| Transistors | 266 | 82 | 165 | 180 | 35 |
| Memristors | NIL | NIL | NIL | NIL | 52 |
| Technology (ηm) | 180 | - | 90 | 65 | 45 |

In the following Table 4, the proposed Flash ADC performance is compared with other existing work and can be found to have better results in terms of power, speed, size, and number of transistors used, for which, by using a 1V power supply, the power dissipation was found to be 1.23 mW.

## 5. Memristor - CMOS Integration

Memristive devices can be fabricated on CMOS silicon wafers through processes compatible with Back-End-Of-Line (BEOL) integration, enabling hybrid architectures for ultra-low-power Flash ADCs meant for AI applications.

In this approach, CMOS circuits are first fabricated using standard silicon technology, followed by the deposition of Memristive Metal-Insulator-Metal (MIM) stacks on the upper metal layers without disturbing transistor performance.

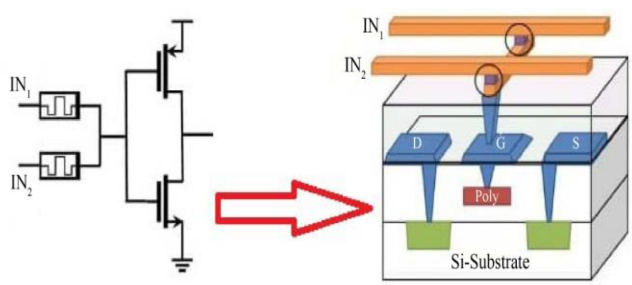



**Fig. 27 Memristor-CMOS integration**

This vertical CMOS–memristor integration, as shown in Figure 27, enables reduced power consumption, compact area, and reconfigurable operation, making it well-suited for energy-efficient Flash ADCs and in-memory computing architectures for AI applications.

## 6. Conclusions

Due to the advantages of Memristor capable of Nano-size dimension which are inherent to replace traditional CMOS, memristors can be used in place of resistors whose value can easily be programmed instead of generating a fixed resistance voltage which is very difficult to fabricate in order to generate the voltage reference, hence can be used for Artificial Intelligence (AI) based applications for reprograming feature is inherent, also it can be used in comparators to reduce the power dissipation, as well as can be used in the design of digital logic gates which reduces the number of components when compared with the traditional CMOS approach, hence with this Approach memristor based Flash ADC was implemented, the circuit schematics were made out using VTEAM model for Memristor in Verilog-A and Simulation results were obtained using the Cadence Virtuoso design environment, from the results the ADC power consumption was found to be 1.23 mW using a supply voltage of 1 V and the delay time was 18.8 ns, hence this proposed Flash ADC reduces the number of transistors to Half when compared with the traditional CMOS technology.

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