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Review Paper

A Review/Steady State Analysis of SEPIC Topologies in the Context of EV Charging Applications

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Abstract - *A SEPIC converter (Single-Ended Primary Inductor Converter) is an ideal converting device that converts DC to a higher value/lower value, depending on the application requirements. The study focuses on reviewing different SEPIC topologies and considering the application of EV charging. Since the topology can realize a broader bandwidth of power variations and can result in several operation voltage ranges, the SEPIC topology is considered ideal in the context of EV charging. The detailed operation of different topologies is studied, and the resulting operation modes and steady state analysis of the operation modes are also studied. On the basis of the study, a comparison of the desired features with reference to EV application was made, and a conclusion on the basis of the study resulted in the ideal operation realm of the converter.*

Keywords - *SEPIC, Interleaved Converter, Coupled Inductor Converter, Quasi-Resonant Converter.*

1. Introduction

In the present era, where there is paramount priority given to sustainability, the integration of renewable energy systems into the grid and their associated research are gaining momentum. The reliance on fossil fuel-based systems is increasingly changing; owing to these reasons, renewable energy systems and their functionality in green energy systems are gaining momentum. Power converters are a dominant factor in the implementation of renewable energy systems. DC-DC power converters are particularly used for a number of applications with combined renewable energy systems. Among all the different DC-DC converters, the Single-Ended Primary Inductor Converter, also known as SEPIC, is of particular importance, owing to its unique feature to have an output voltage in different ranges, which is either higher, lower, or equal to the value compared to the input voltage. [1, 2]. SEPIC Converters applications will have added interest if power applications are non-isolated. Due to the wide range of applications, primarily in renewable energy systems, SEPIC Converter topologies are of particular interest. The conventional SEPIC Topologies utilize two inductors, which makes the inductor ripple current two-fold. [3]. Like any other power electronic converter, the power available across the input of the converter is provided to passive components in the configuration, which includes an inductor and a capacitor. Power is exchanged between the components, which further results in the production of the energy either greater than, equal to, or less than the available input.

The studies currently available have discussed the design of SEPIC converter and their performance in renewable energy systems; however, there remains a gap in the comprehensive evaluation of SEPIC topologies in the context of EV Charging applications. Most of the prior works focus on general renewable integration, while very few concentrate on unique challenges posed by EV chargers, which include variation of input voltages, requirement of high efficiency, and other related design needs/requirements. The available reviews primarily gives importance to isolated converter topologies, leaving a lack of comprehensive understanding of how the SEPIC topologies work in EV charging applications. [1-3].

The novelty of the research primarily lies in the focused analysis of different SEPIC topologies, on steady state analysis, modifications to improve the efficiency of the system, ripple reduction, passive component stress, etc. The paper bridges the gap and hence provides a comparison of several critical parameters on the SEPIC topologies [1, 2].

A systematic and detailed literature search was conducted using available databases, including IEEE Explore, Scopus database, etc. The study primarily focused on the applications of EV charging. The papers on the selected application were compared, and the steady state analysis was considered for the development of the paper. Studies that are not related to SEPIC EV charging and those from non-peer-reviewed journals were removed/filtered.

The key terms given below will give an in-depth understanding of the context.

Single-Ended Primary Inductor Converter (SEPIC): It is a converter that provides an output voltage in different variations, either higher than, equal to, or lower than the input voltage.

DC-DC Converter: A device capable of converting DC voltage. This converter can be a Buck, Boost, SEPIC, Cuk, etc.

Bridgeless SEPIC: A SEPIC topology that does not have an input bridge rectifier to reduce conduction losses and to have better efficiency.

Steady-State Analysis: Analysis of the circuit behavior after all transients have been settled, with constant operating conditions.

Interleaved SEPIC: A topology where multiple SEPIC topologies operate out of phase with each other, suitable for high-power EV charging applications.

Coupled Inductor SEPIC: A topology where magnetically coupled inductors are utilized for improved efficiency and performance.

2. Types of SEPIC Topologies

2.1. Conventional SEPIC Converter

One of the prime reasons why SEPIC Topology is adopted for EV charging applications is its high efficiency and the fact that the input ripple current in the configuration is relatively low. Compared to the counterpart Cuk converter, the electrical stress on the SEPIC Converter is less, and the conversion rate is appropriate and desired.

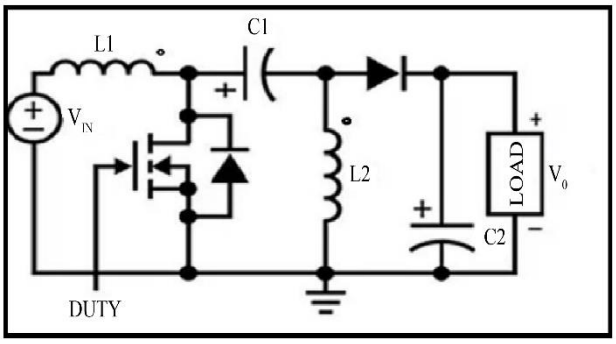

Fig. 1 Model of Conventional SEPIC Converter [4]

The converter configuration has a power switch, typically a high-frequency switch, 2 inductors, named as L1 and L2, one capacitor, which is referred to as the coupling capacitor and is named as C1, and an output capacitor, C2, to filter out signals that are not desired. The detailed analysis of the converter is presented below. Mode 1 operation of the converter is characterized by the operation in the range (0<t<DTs).In the specified range, Ts stands for switching time period. During the time interval mentioned, the pulses provided to the converter for its operation are high. As the pulse is high, the power switch connected will be in the on state, wherein the inductor, named as L1, gets charged by the input supplied, and inductor L2 will also start to charge with the help of energy released from capacitor C1. The freewheeling diode will not get turned on at this point in time, and the value of Vo will be kept within the limits by the capacitor C2.

Mode 2 operation of the converter is identified in the operation range when the instantaneous time lies between the product of the duty ratio and the switching time. When the pulses given to the inductor are in the lower state, the switch connected will be in the non-conducting mode, which results in the energy stored in the inductor being released to the load via the diode, and the capacitors get charged at this point in time. The diode D gets turned on in this mode of operation, owing to the fact that the inductor L2 changes the direction of current to oppose any further change in the current. The discharge of current will be via the capacitor C2 as shown in Figure 2 [3].

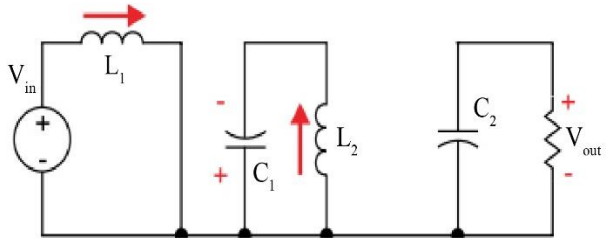

Fig. 2 Operational diagram when switch S1 is on [4]

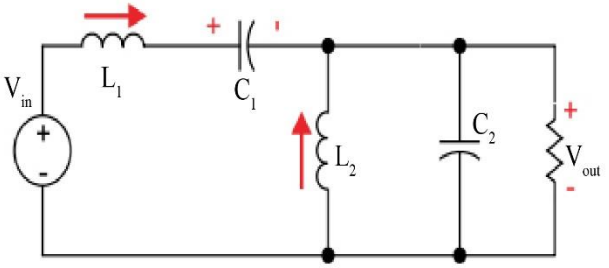

Fig. 3 Operational diagram when switch S1 is off [5]

The output voltage obtained in a conventional SEPIC Topology can be represented using the equation given below.

$$Vo = \frac{D}{1-D} * Vin \quad (1)$$

As per what is given in (1), Vo represents the value of voltage at the output side. D represents the duty ratio of the SEPIC, and Vin is the voltage at the input of the SEPIC configuration. The value of D is given below in (2)

$$D = \frac{Vo+Vd}{Vin+Vd+Vo} \quad (2)$$

2.2. PWM Switch Model of SEPIC Converter

The paper focuses on the DC analysis of the SEPIC topologies, and for the conventional converter, the adoption of Vorperian's PWM Switch Model is the best practice for developing the DC analysis equations. Some minor manipulations have to be implemented to adopt the model in practice, which includes rearranging the capacitor C1 and the Inductor L2 as shown in Figure 4.

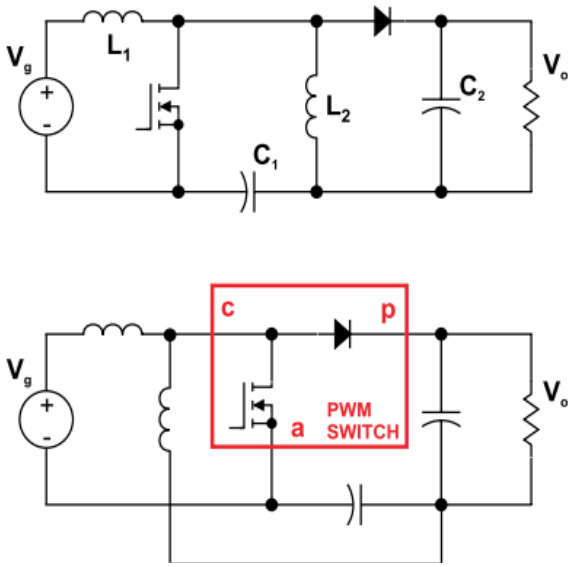

Fig. 4 PWM switch model [5]

As seen in Figure 4, the capacitor C1 is pulled down to the bottom branch, and the inductor is dragged to the extreme left of the converter configuration for the DC analysis of the circuit. For conducting DC analysis, the signal source is set to zero volts, inductors are considered to be short circuits, capacitors are assumed to be open circuits, and KVL equations are adopted for the analysis. Figure 5, as given below, shows the analysis model of the SEPIC (DC). According to what is given in illustration 5, the PWM DC Switch model is incorporated, which has a representation of a 1: D transformer in place for the converter. Developing the KVL equation in the outer loop results in an equation as given below

$$Vg + Vo - \frac{1}{D} Vo = 0 \quad (3)$$

In Equation (1), Vg is the voltage at the input side of the converter, and D represents the duty ratio of the SEPIC. Re-arranging the equations results in Equation (2), which is given below as

$$Vg = \left(\frac{1}{D} - 1\right) Vo = \frac{D}{D'} \quad (4)$$

From equation (2), the DC gain is given as

$$V0 = \frac{D}{D'} * Vg \quad (5)$$

Equation (3) implies the ability of the SEPIC Converter to effectively boost or buck the converter voltage. In Equation (3), D' refers to the complementary duty cycle, which is the duty cycle corresponding to when the converter is off.

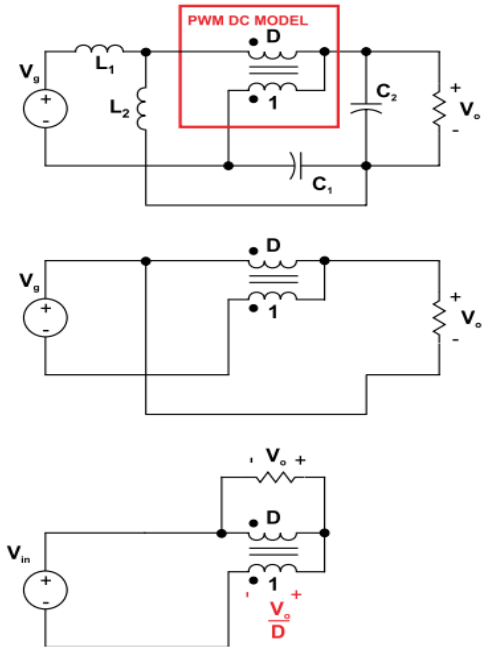

Fig. 5 DC analysis model [5]

2.3. SEPIC Converter-Bidirectional

A bidirectional converter is primarily employed in applications that require bidirectional energy transfer between DC buses. A bidirectional converter with a coupled inductor is presented in Figure 6 [6].

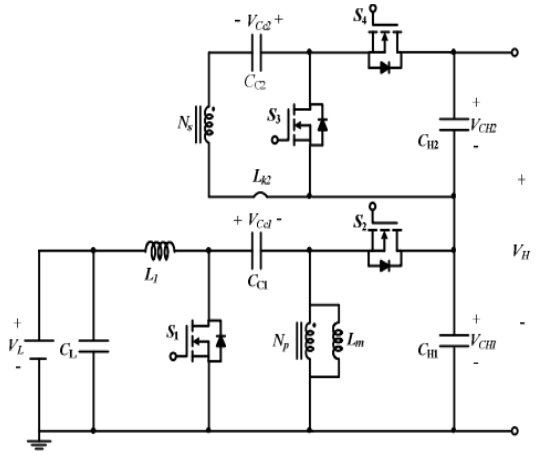

Fig. 6 Bidirectional SEPIC converter [6]

The converter has a high conversion ratio, and the resulting inductor energy (leakage) was found to be recycled in all the cases in the adopted converter, which includes

charging and discharging modes. Voltage stress across the converter was found to be significantly less owing to the clamping of the circuit, which will further result in attaining high efficiency of the circuit [6]. The conversion efficiency of the converter was found to be around 94.3% at the discharging mode of operation. So, the analysis in the paper is focused on the DC analysis of the converter in the discharging mode. The analysis of the converter is done by considering certain assumptions as given below: All passive components are taken to be without any losses or in other words considered to be ideal however inductance (leakage) value is considered to be non-ideal, considering the passive inductor/capacitive elements are large enough will result in constant voltage across capacitor configuration and constant current across inductor configuration. The illustration given below is in the discharging phase.

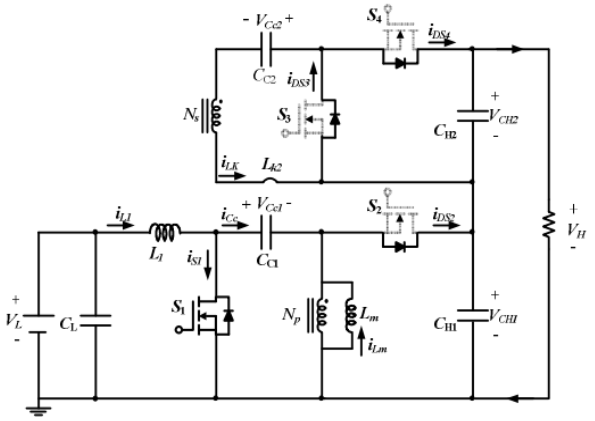

Fig. 7 Converter configuration in discharge mode [6]

As seen in Figure 7, Switch S1 is considered the main/primary switch, and switches S2, S3, and S4 were considered rectification diodes. The switching period considered for the analysis is Ts. The full operation of the converter is divided into 7 phases, and a detailed analysis is given below.

Mode 1 [t0, t1]: This mode is characterized by the turning on of the switch S1 and turn off of the switching diodes SD2 and SD3, wherein the switching diodes, SD4 will be on at this point of time current through the converter icc and ids4 drops in this time interval, is1 will try to reach the magnitude of iL1 at this point of time, when time t=t1.

Mode 2 [t1, t2]: In this mode of operation, the first switch is in the on state, where in the diodes Ds2 and DS4 are in the open state and diode DS3 is in the closed state. The input side continues to provide current to the inductor, which results in an increase in current through it. The power released from capacitor Cc1 and Lm is transferred to CC2. The current ILm becomes zero at the time instant of t2. The characteristic operation analysis equations applicable in this scenario are given below.

$$\text{VLm} = \text{-Vcc1} = \text{VL- VL1} = \frac{-Vcc2}{n} \quad (6)$$

$$\Delta\, iLm = \frac{VL-VL1}{Lm}\,(t2-t1) = \frac{-Vcc2}{nLm}\,(t2-t1) \quad (7)$$

Mode 3 [t2, t3]: At this mode of operation, the current through the inductor Lm continues to increase rapidly. The corresponding equations of the mode's operations are given below.

$$\text{VLm} = \text{-Vcc1} = \text{VL- VL1} = \frac{-Vcc2}{n} \quad (8)$$

$$\Delta\, iLm = \frac{VL-VL1}{Lm}\,(t3-t2) = \frac{-Vcc2}{nLm}\,(t3-t2) \quad (9)$$

Mode 4 [t3,t4]: At Mode 4 switch, S1 continues to be in the on state, the switching diode DS4 is turned off at this point in time, whereas switching diodes DS2 and DS3 are turned on. The leakage inductance energy was released to capacitors CC2 and CH1. The voltage across inductor Lk2 will be a clamped voltage, which is given as

$$V_{LK2} = V_{CC2} + V_{CH1} \quad (10)$$

Mode 5 [t4,t5]: At mode 5, Switch S1 is turned off and switching diode DS3 is turned on; the other switching diodes DS2 and DS4 are turned off. The inductance (leakage) will continue to receive energy as the current through the switch IDS4 increases and the current through IDS2 decreases. At the end of time t=t5, the current IDS2 decreases and reaches zero [6].

$$\text{VLm} = \text{VL} - \text{VL1} - \text{Vcc1} = \text{VCH1} = \frac{\text{VCH2}-\text{VCC2}}{\text{n}} \quad (11)$$

$$\Delta\, iLm = \frac{VCH2-Vcc2}{nLm}\,(t5-t4) \quad (12)$$

Mode 6 [t5,t6]: Mode 6 is characterized by the turned-off mode of switch S1 and switching diodes DS2 and DS3, and the turned-on state of switching diode DS4. The current iDS4 and iLm decrease at this point in time. Towards the end of the operation, the current ILm becomes equivalent to zero. The corresponding applicable equations of the mode are given below

$$\text{VLm} = \text{VL} - \text{VL1} - \text{Vcc1} = \text{VCH1} = \frac{\text{VCH2}-\text{VCC2}}{\text{n}} \quad (13)$$

$$\Delta\, iLm = \frac{VCH2-Vcc2}{nLm}\,(t6-t5) \quad (14)$$

Mode 7 [t6, t7]: During this mode of operation, which is similar to that of mode 6, except for the operation of inductor Lm, the current through the inductor increases but in the reverse direction. At the end of this mode, the switch S1 is turned on, and the cycle repeats itself.

$$VLm = VL - VL1 - Vcc1 = \frac{VCH2-VCC2}{n} \quad (15)$$

$$\Delta\, iLm = \frac{VCH2-Vcc2}{nLm}\,(t7 - t6) \quad (16)$$

By applying the Volt-second balance principle and hence implementing the equation for the voltage across inductor Lm, results in the following equation,

$$\frac{1}{Ts}\int_0^{Ts} VLm\, dt = 0 \quad (17)$$

which further implies equivalent to

$$\sum_{t0}^{t7} \Delta\, iLm = 0 \quad (18)$$

Substituting equations (6), (8), (11), (13), and (15) into Equations (17) will further result in obtaining the conversion ratio of the adopted converter, which is represented using the equation as given below [6],

$$\text{Conversion ratio} = \frac{VH}{VL} = \frac{n+D}{1-D} \quad (19)$$

2.4. Coupled SEPIC Converter

The primary difference between a SEPIC converter, which is a conventional one, and the one with a coupled inductor configuration is that in the latter configuration, the inductors are wound on the same core, which tends to reduce the bulkiness of the circuit. The operation of the model is the same as that of the conventional SEPIC, which can be discussed in 2 modes, which are mode 1 and mode 2. Mode 1 has the operation when the switch SW is on and the inductors are wound on the same core as L (the coils are named as L1 and L2 in analysis equations, respectively, from left to right). Mode 2 is recognized by the turning off of the switch SW, which results in the discharging of capacitor CAC, resulting in the availability of current through the load [7].

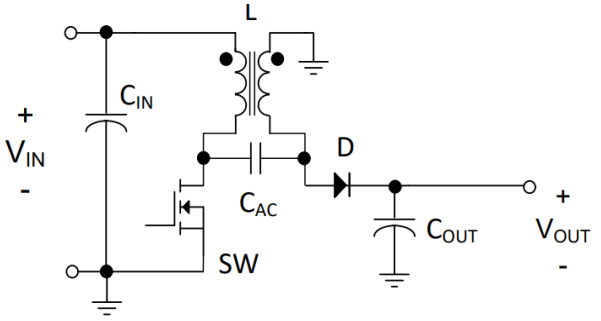

Fig. 8 Circuit Diagram of coupled Inductor SEPIC [8]

The equations corresponding to the mode 1 operation of the SEPIC Converter with a coupled Inductor are given below,

$$L1\frac{diL1}{dt} + M\frac{diL2}{dt} = Vi \quad (20)$$

$$L1\frac{diL2}{dt} + M\frac{diL1}{dt} = Vc1 \quad (21)$$

$$C1\frac{dvc1}{dt} = -iL2 \quad (22)$$

$$C2\frac{dvc2}{dt} = -\frac{vc2}{RL} \quad (23)$$

Mode 2 operation equations corresponding to the coupled inductor configuration are given below.

$$L1\frac{diL1}{dt} + M\frac{diL2}{dt} = Vi - VC1 - VC2 \quad (24)$$

$$L2\frac{diL2}{dt} + M\frac{diL1}{dt} = -Vc2 \quad (25)$$

$$C1\frac{dvc1}{dt} = iL1 \quad (26)$$

$$C2\frac{dvc2}{dt} = -\frac{vc2}{RL} + iL1 + iL2 \quad (27)$$

[7].

For designing a converter with a coupled inductor configuration, the following parameter calculations and determinations are desired: input voltage range, nominal output voltage range, maximum output current, maximum output power, desired switching frequency, and converter IC selection [8].

However, using a coupled inductor SEPIC converter, an optimal output can be attained by ensuring an appropriate adoption of the coupling capacitor when using tightly coupled inductors, as the tightly coupled inductors might result in high ripple currents in the input as well as in the output side. SEPIC configuration works best with PV panels, especially the coupled inductor configuration [9]. In fact, SEPIC configuration is one of the top configurations that works best with the P & O method of the MPPT system when compared to its counterparts, and hence, it obtains an optimized output. In fact, SEPIC topologies are one of the best topologies that work very effectively with PV systems [10].

2.5. Interleaved SEPIC Converter

An interleaved configuration of the SEPIC Converter is developed by connecting individual SEPIC Configurations in parallel. These topologies can work in both continuous and discontinuous modes of operation. If this topology is adopted, one of the critical factors, voltage stress, is considerably reduced due to interleaving. This sort of model is used for operations requiring low voltage, whereas the power requirements are high. Some of the advantages of the interleaved configurations include reduced losses while the converter is kept in conduction. For any multi-level SEPIC topologies, a phase shift of signals is desired to have effective operation of the levels implemented. An example of a 2-stage interleaved configuration is depicted below in Figure 9 [11].

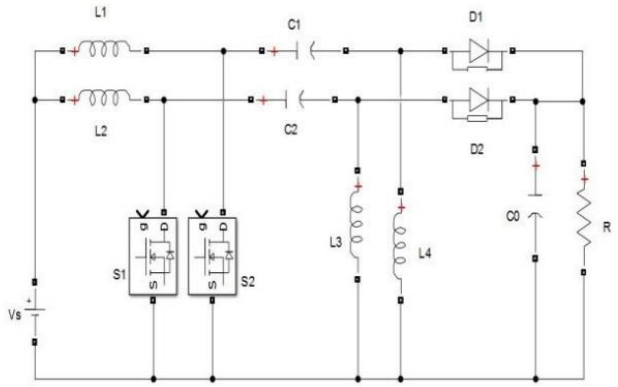

Fig. 9 2-stage SEPIC Topology [11]

As seen in Figure 9, two stages of the conventional SEPIC phase are shifted by PWM input signals with a phase difference of 180 degrees, which are implemented. Compared to the traditional SEPIC topology, the converter has 2 switches, inductors (2 in number), capacitors (2 in number), and diodes (2 in number), primarily to ensure efficient operation of the converter. The analysis is concentrated on the continuous operation phase of the converter as given below. However, it is also pertinent that the converter can also operate in non-continuous mode as well [11].

Mode 1 operation: Figure 10 shows the working in mode 1. At this operation, S1 will be on and S2 will be off. The connected passive element capacitor starts to get charged in this mode. Two diodes are active at this mode; however, D1 is said to be closed, and D2 is in open mode. The inductors connected to the L1 and L2 configurations start to discharge to the load in this mode. From the illustration, considering the input current as i1 and considering the loop which includes the input voltage source, inductor L1, capacitor C1, and the load, the steady state DC equation can be written as [12],

$$\mathrm{Vin} - \mathrm{L1}\frac{\mathrm{di1}}{\mathrm{dt}} - \mathrm{Vc1} - \mathrm{I1R1} = 0 \qquad (28)$$

Considering loop 2 in Figure 12, which includes inductor L2 and the output capacitor C2, assuming the current through the loop can be written as below,

$$L2\ \frac{di2}{dt} = VC2 \qquad (29)$$

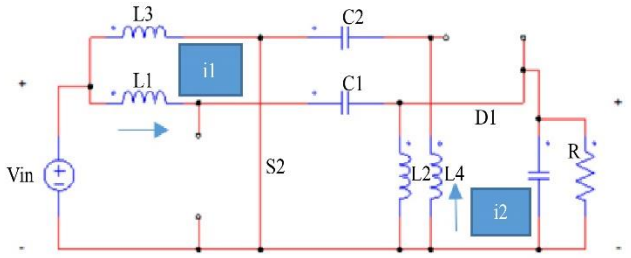

Fig. 10 Model 1 operation of 2-stage SEPIC Converter [12]

Mode 2 Operation: As seen in Figure 11, switches S1 and S2 are both turned on in this mode. The inductor L1 is storing energy at this point in time as the input energy starts to increase. In this context, the steady state equation from the input side can be written as given below.

$$Vin - L1\frac{di1}{dt} - VS1 = 0 \qquad (30)$$

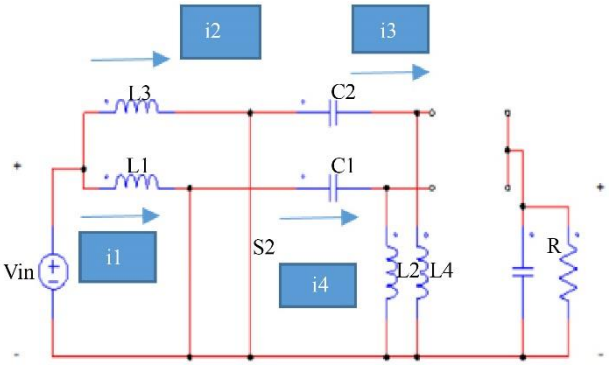

Fig. 11 Mode 2 operation of 2-stage SEPIC Converter [12]

Considering the current through the inductor L3 as i2 and taking into account the loop which consists of the input voltage vin, inductor L3, and switch S2, the corresponding equation can be written as

$$Vin - L3\frac{di2}{dt} - VS2 = 0 \qquad (31)$$

Mode 3 Operation: In this mode of operation, one of the switches, S1, is in the closed state, and switch S2 is in the open state. The passive element, particularly L1 and L2, is said to be in charging mode, and the connected inductors L3 and L4 are said to be in discharging mode. The diodes connected to the output side, D1, are not turned on, whereas diode D2 is turned on.

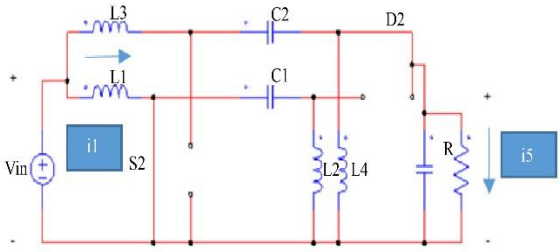

Fig. 12 Mode 3 Operation of the converter

Considering the loop which includes the inductor L1, the Vin, and the closed switch S1, the current through the inductor is specified as i1.

$$\mathrm{Vin} - \mathrm{L1}\frac{\mathrm{di1}}{\mathrm{dt}} - \mathrm{VS1} = 0 \qquad (32)$$

Considering the output loop, which includes closed switch diode D2, output load, and inductor L4, the steady state equation can be written as,

$$-VL4 - VD2 - I1R1 = 0 \quad (33)$$

Mode 4 Operation: Mode 4 is characterized by the turn off of switches S1 and S2. All the inductors start to discharge, delivering the current to the load.

Considering the loop which includes inductor L4, Diode D2, and the load connected, the steady state equation can be written as [12],

$$-VL4 - VD2 - I1R1 = 0 \quad (34)$$

The combined output voltage of the 2-stage SEPIC is given as,

$$Vout = \frac{D}{1-D} * Vin \quad (35)$$

All the terms of equation (35) are discussed in the statements given previously.

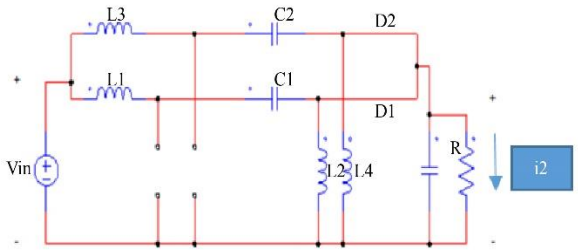

Fig. 13 Mode 4 operation of 2-stage SEPIC Converter [12]

Using SEPIC Configuration, even more levels can be constructed (refer to Figure 14), which further increases conversion efficiency and can result in a reduction of voltage stresses. A typical model of a 4-level interleaved SEPIC configuration, with increased conversion efficiency and reduced voltage stress, is presented in Figure 16, which has an output voltage multiplier configuration connected (doubler), which can further result in increasing the conversion efficiency. Interleaving can result in the construction of topologies with two-level, three-level, or even four-level. As the number of levels increases, the voltage stress, switching losses, and other parameters that adversely affect the performance can be optimized [13].

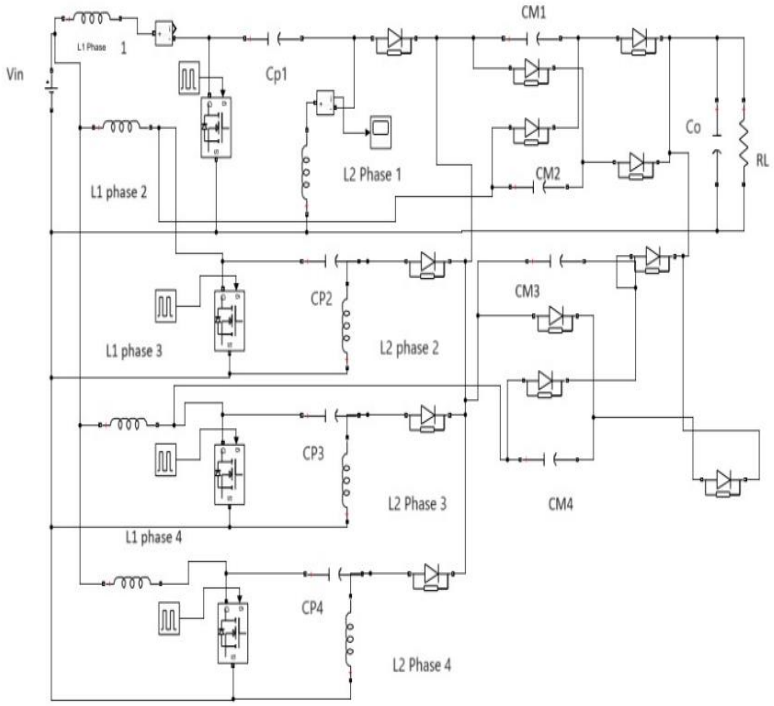

Fig. 14 4 Level Interleaved configuration of SEPIC with voltage multiplier

SEPIC configuration can also be adopted for an onboard EV charging system, wherein a multi-level PF-based converter topology can be implemented. These types of SEPIC Converters are primarily used to eliminate/minimize the harmonics in the EV charging configuration. Switches in a 2-stage SEPIC topology experience a 50% reduction in current stress compared to the conventional converter, making the converters unique and efficient [14].

2.6. Interleaved Isolated SEPIC Converter

For low-power applications, SEPIC working in non-continuous mode is normally desired. In this specific case, the converter is a unidirectional converter. The converter presented has many stages implemented, which include a full diode bridge converter as the first stage, and connected to it in the second stage is an isolated and interleaved SEPIC Configuration [15].

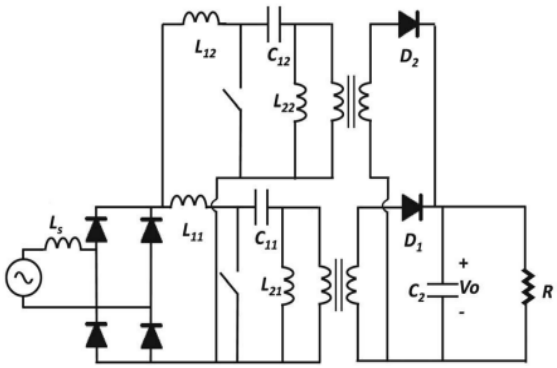

Fig. 15 Interleaved Isolated SEPIC PFC Converter (bridged) [15]

Interleaving is incorporated, wherein the power division of several modules is implemented. Due to interleaving, power devices of lower rating can be incorporated, allowing effective reduction of overall converter size. SEPIC inductances were significantly reduced owing to the fact that they are magnetically coupled, thereby reducing converter size and increasing efficiency.

The model had a bridged configuration, which tends to further increase the complexity of the circuit. In order to further reduce the complexity and to be useful for onboard EV charging applications, a modified model, which is a bridgeless model, can be adopted, as given in Figure 16. The model is developed by combining two SEPIC topologies in parallel and hence comes under an interleaved configuration.

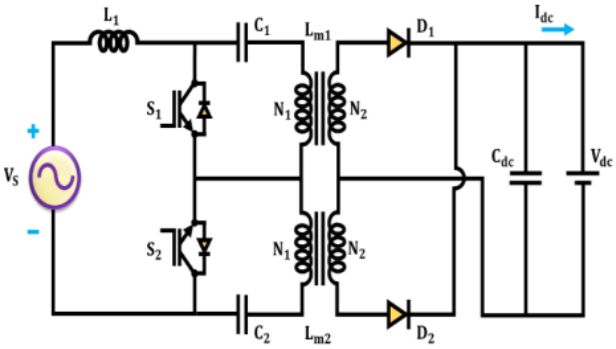

Fig. 16 Bridgeless Isolated SEPIC Converter [15]

The switching operation consists of 2 switches operating separately in positive and negative half cycles. When the converter is working in the positive half cycle, the switch S1 and Diode D1 are closed, wherein the second switch S2 is in the open state. In the next half cycle, the operation is reversed, and switch S2 and Diode D2 will be in the closed state. The detailed operations in different modes are discussed below.

Mode 1 [t0-t1]: At this mode of operation, switch S1 is in the on state, and the inductor Lm1 stores the energy that was dissipated by the capacitor C1. This is represented in Figure 17.

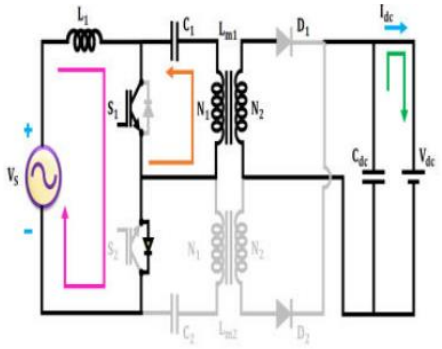

Fig. 17 Mode 1 operation of the Bridgeless Isolated converter

The inductor shown in Figure 17, Lm1, primarily stores energy, which is dissipated by the capacitor C1. The current through the inductor Lm1 is given using the formula.

$$iLm1(t) = ILm1\ (t0) + \frac{Vc1}{Lm1}\ (t - t0) \tag{36}$$

The input current through the inductor Li is specified using the equation given below.

$$\text{I Li (t)} = I\ Li\ (to) + \frac{Vin}{Li}\ (t - t0) \tag{37}$$

Using Equations (35) and (36) and simplifying the equations resulted in Equation (37)

$$is1(t) = i\ Li(t) + iLm1\ (t) = ILi\ (t0) + I\ Lm1(t0)\ \frac{Vin}{Li\ //Lm1}\text{(t-t0)} \tag{38}$$

Mode 2 [t1-t2]

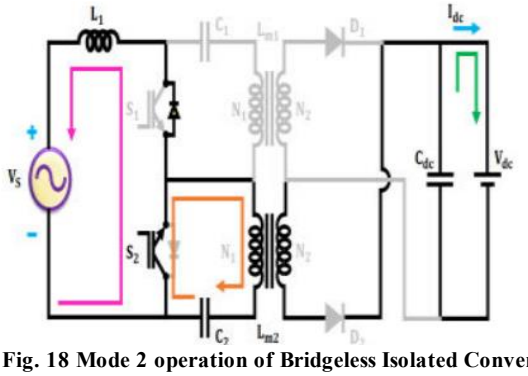

Fig. 18 Mode 2 operation of Bridgeless Isolated Converter

Unlike the operation in mode 1, the switch S1 is off throughout the operation, and the diode D1 conducts due to the flow of current iLi and iLm1. The current through the diode D1 and DS2 will be together, as given in the equation below.

$$Vin\,(t)\,D + (Vin(t) - Vc1 - nVdc)\,D1 = 0 \quad (39)$$

$$Vc1 - nVdc = \frac{D}{D1}\,Vin \quad (40)$$

As D+D1 ~= D (41)

The current through the inductors is represented by the equations as given below.

$$I\,Li(t) = ILi(t0) + \frac{Vin}{L1}\,DTs + \frac{Vin - Vc1 - nVdc}{L1}\,(t - t1) \quad (42)$$

$$ILm1(t) = ILm1\,(t0) + \frac{Vin}{Lm1}\,DTs + \frac{Vin - Vc1 - nVdc}{Lm1}\,(t - t1) \quad (43)$$

Mode 3 [t2-t3]

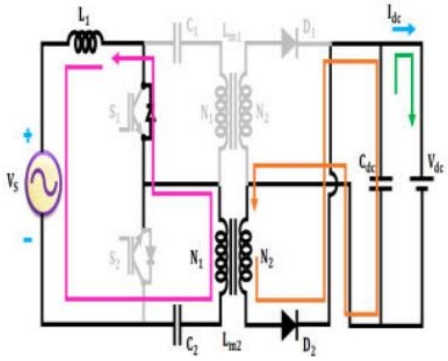

Fig. 19 Mode 3 operation of bridgeless isolated converter

Switch S1 is in the open state, and at this point in the instance, the current through Lm1 is discharged. Diode D1 was not conducting at this point in time. The current through the inductors is represented by the equations given below.

$$I\,Li(t) = I\,Li(t0) + \frac{Vin}{Li}\,DTs + \frac{Vin - Vc1}{Li}\,(t - t2) \quad (43)$$

$$iLm1\,(t) = 0 \quad (44)$$

For the time interval as given as t2 ≤ t ≤ Ts

Is1 =0, iD1 =0 (45)

2.7. High-Frequency Quasi-Resonant SEPIC Converter

A modified converter with characteristics of SEPIC Topology and Quasi-resonance was implemented in the configuration. The system has incorporated the ZCS or ZVS method, which can further result in better operational characteristics of the converter. One of the primary differences between the conventional and modified quasi-resonant topology is the placement of components and sizing parameters. This type of converter is designed to be operated even in the megahertz range, which makes its operations ideal. In order to comply with the ZVS/ZCS mechanism, bulk inductors are used just like a conventional SEPIC topology. The capacitors connected in the topology are connected in parallel with switches and diodes with an additional inductor (resonant), which is connected in a serial configuration to have ZVS for the converter configuration [17]. The configuration given below has no bulky inductor configurations; there are inductors (resonant) implemented with one additional inductor, which aids resonant inversion, whereas the other aids resonant rectification [17].

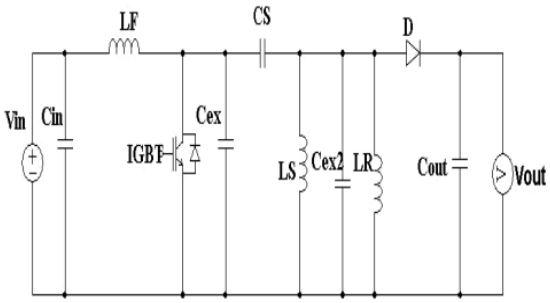

Fig. 20 Quasi Resonant SEPIC Converter [17]

Mode 1 operation: As per the mode 1 operation, the switch S1 will be on, and the current in the input side passes through the inductor LF and the capacitor Cex. The diode D will be turned off, and no current will pass through Cout. The capacitor cx2 and the inductor LR start to charge at this point in time.

$$i\,Lf\,(t) = i\,Lf(0) + \frac{Vin}{Lf}\,t \quad (46)$$

The current through the inductor Ls and LF also increases at this point in time.

$$i\,Ls\,(t) = i\,Ls(0) + \frac{Vcex}{Ls}\,t \quad (47)$$

Mode 2 operation: The switch in this mode of operation turns off. The diode Dis is turned on at this point in time; hence, the current passes through Cout. Lr and Cex2 start to oscillate at this mode of operation.

$$iLr(t) = I\,peak * \sin(wrt) \quad (48)$$

$$i\,D1(t) = I\,peak * \sin(wrt) \quad (49)$$

Mode 3 operation: The inductors store energy, and the energy gets released at this mode of operation. The diode D1 starts conducting, and the current passes through the load [18].

$$i\,Lf\,(t) = iLf(t)e^{\frac{-t}{\zeta}} \quad (50)$$

$$\text{Where } \zeta = \frac{LF}{R\ load} \quad (51)$$

3. Recent Advances in the SEPIC Topologies

Improved SEPIC topologies incorporating Power factor correction systems to improve the efficiency of the system in general are quite popular nowadays, and this is also in compliance with IEC 61000-3-2 standards. The method provides good transient response, and steady state response is comparable with other leading topologies commercially available, making the system quite efficient altogether [19].

SEPIC-based EV charging must also be controllable; in this context, controllers like PI, PID, etc., provide operations with excellent response and minimize errors [20]. Bridgeless SEPIC topologies with PFC ensure that the conduction losses in the system implemented are minimal and maximizes efficiency. This type of system is ideal for high-performing EV charging stations [16]. Fuzzy logic /AI implementation on SEPIC topologies makes the systems smart and automated, where a constant voltage/current charging methodology can be adopted for charging the electric vehicles powered by modern methods like fuel cells. This type of approach enhances efficiency and adaptability with varying load conditions, making the system ideal [21].

4. Design Considerations for EV Charging

The efficient utilization of SEPIC topologies for EV charging is critical for maximizing various critical parameters like voltage gain and efficiency. To address these issues, various critical design considerations have to be considered.

4.1. Input Voltage Range and Power Rating

EV chargers normally operate in a wide voltage range, normally ranging from 90-265 V AC for grid-connected systems, and 200-450 V DC for renewable integrated systems. Power ratings for on-board chargers range from a very few KW ratings to hundreds of KW ratings for off-board chargers.

4.2. Component Selection and Stress Analysis

Efficient selection of inductors and capacitors in the topologies is required to minimize the ripple current and to reduce losses. Semiconductor devices like diodes and switches must operate at a rating much higher than nominal voltages and currents to have safe operation.

4.3. Efficiency and Thermal Management

High efficiency is of paramount importance for the efficient charging of EVs. The strategies that can be adopted include interleaving, soft switching, and coupled inductor configurations, etc., that would reduce switching and conduction losses. Appropriate heat dissipation systems, like heat sinks, are also required for thermal management.

4.4. Power Quality and Compliance with Standards

For grid-connected converters, connection to the Power factor correction systems is absolutely required, primarily to comply with standards IEC 61000-3-2.

4.5. Control Strategy

Any control strategy to effectively control the operation can be adopted, which includes PI, PID controller, etc.

The design targets and associated considerations for the systems and the converter, specifically, are given below in tables.

Table 1. System-level targets for Onboard Vs off-board chargers

Criteria	On-board Charger	Off-Board charger (Fast charging)
Input AC Voltage	Rms voltage of the range 90 to 265 V, frequency 50/60 Hz	3 phase 380-480 V rms (50/60 Hz)
DC Source voltage	200-450 V	600-1000 V (from rectifier/PFC)
Rated Power	3.3-11 KW	50-350 KW
Switching frequency	80-250 KHz	50-150 KHz
Current ripple for input L	15-30% of input IL average	10-25% of input IL average
Output voltage ripple	≤ 1% Vout (CC), ≤ 0.5% Vout (CV)	≤ 0.5%-1% of Vout

Table 2. Numerical values of components for SEPIC Variants

SEPIC Variant	Switching frequency	Inductor per phase	Capacitor per phase
Conventional SEPIC (1 phase)	100 KHz	250-350 µH	2-4 µF
Coupled Inductor SEPIC (1 phase)	150-200 KHz	120-200 µH	1-2 µF
Interleaved SEPIC (2 Phases)	120-180 KHz	120-180 µH	1-2 µF per phase
Interleaved Isolated SEPIC (2-4 Phases)	100-150 KHz	80-150 µH/phase	1-1.5 µF per phase
Quasi Resonant SEPIC (1-2 Phase)	250-500 KHz	60-120 µH/per phase	0.68-1.5 µF

As per Table 2, the variation of numerical values that can be implemented in the model as per the need, is given; the simulation results were obtained by adopting the numerical values as given in Table 2.

5. Results and Discussions

Simulations of these converters were done using the MATLAB Simulink platform, and the prototypical data values were used to attain the efficiency and voltage gain calculations of the corresponding converters. As per Table 3, the conventional SEPIC Converter has an efficiency of around 88%, voltage gain is found to be moderate, and switching losses were found to be relatively high at around 20 W, primarily due to the double inductor configuration and non-availability of advanced soft switching techniques. For these reasons, the configuration is not quite suitable for advanced EV charging applications.

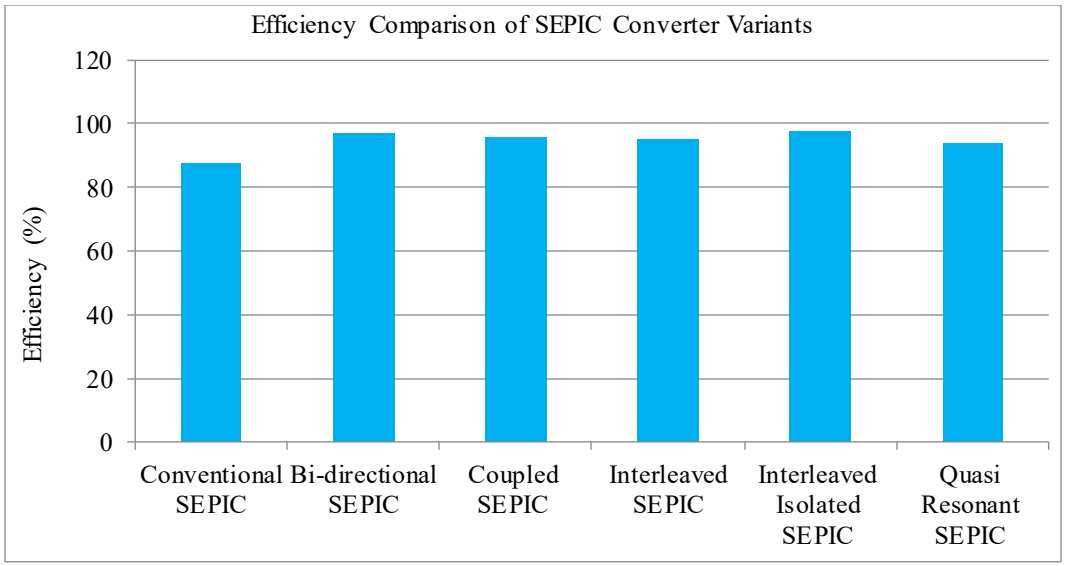

Fig. 21 Efficiency comparison of different SEPIC Topologies

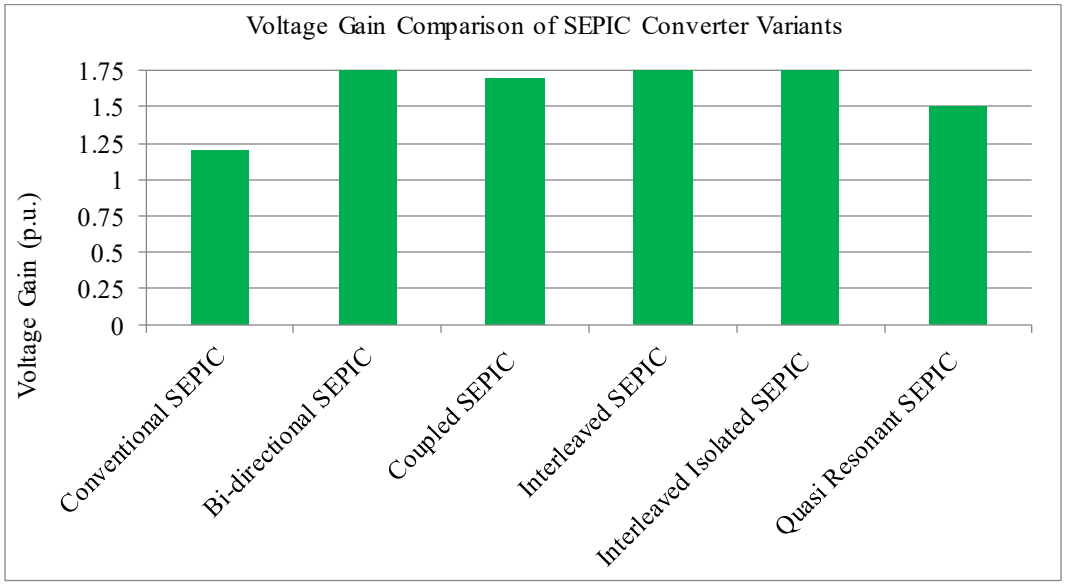

Fig. 22 Voltage gain comparisons of different SEPIC Topologies

Table 3. Efficiency, voltage gain, and switching losses data

Sl. No	Converter Type	Efficiency (%)	Voltage Gain(p.u)	Switching losses (W)
1	Conventional SEPIC	88	1.2	20
2	Bi-directional SEPIC	97	1.8	10
3	Coupled SEPIC	96	1.7	12
4	Interleaved SEPIC	95	1.75	11
5	Interleaved Isolated SEPIC	98	1.9	8
6	Quasi Resonant SEPIC	94	1.5	15

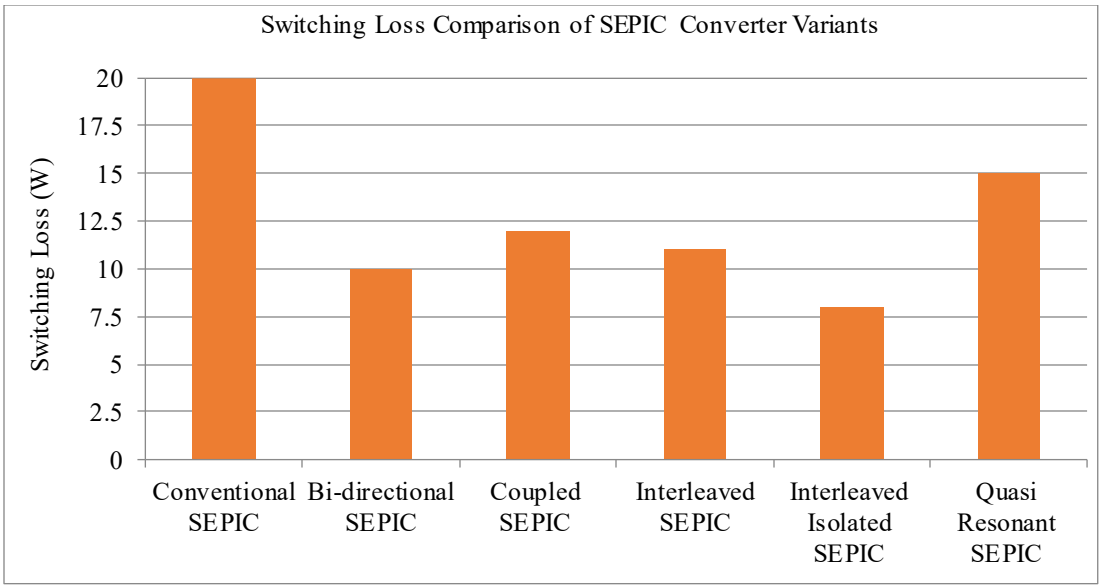

Fig. 23 Comparison of switching losses in SEPIC Topologies

Table 4. Consolidated Comparison of the SEPIC Topologies

Sl. No	Type of SEPIC converter	Efficiency (range)	Features after the study of analysis	Suitability for EV Charging applications
1	Conventional SEPIC Converter	85-90%	Voltage gain, as per the analysis, was found to be moderate. Switching losses were found to be considerable compared to other converters.	Not suitable owing to the considerable losses
2	Bi-directional SEPIC Converter	95-98%	Voltage gain was found to be high, and switching losses were found to be variable, ranging from moderate to less, depending on the controlling techniques implemented.	Suitable for on-board charging, specifically where there is applicability of vehicle-to-grid charging
3	Coupled SEPIC Converter	95-98%	Voltage gain is considerably high, and switching losses were found to be medium.	Suitable for an off-board charging system
4	Interleaved SEPIC Converter	94-97%	Voltage gain is considerably high, and the switching losses are moderate to low, with higher power handling capacity and reduced ripples.	Suitable for an off-board charging system
5	Interleaved Isolated SEPIC Converter	96-99%	Voltage gain is high; however, the complexity is considerable, and switching losses are very low.	Suitable for grid-connected EV Charging systems.
6	Quasi-Resonant converter	92-96%	Voltage gain is medium, and switching losses are found to be moderate	Can be used in the off-board EV Charging

Among the variants, non-isolated bidirectional SEPIC showed the highest performance at 97%. It has a high voltage gain of 1.8, and switching losses were found to be less than 10 W only. Hence, the converter can be used for on-board EV charging applications. As given in Table 4, the following key points can be derived. On the basis of the study in different contexts, different SEPIC topologies can be adopted. In comparison with the modified topologies, the conventional SEPIC converter was found not to be an ideal choice for EV applications. If the EV Charging system is on-board, then bi-directional SEPIC topology can be adopted. If the application is an off-board charging system that is connected to the grid, an interleaved isolated SEPIC topology with galvanic isolation can be implemented. For an off-board charging system that can be connected to a renewable-based system like a PV or WECS system, coupled SEPIC and interleaved SEPIC converters were found to be the ideal selection.

6. Conclusion

A comprehensive simulation-based analysis of different SEPIC topologies was done in the paper, wherein the emphasis on conduction losses, voltage gain, and efficiency was given. The results show that a conventional SEPIC converter topology with an efficiency of around 88% and a moderate voltage gain, which has high switching losses of around 20 W, was found to be quite suitable for EV charging

applications. In this context, the other topologies of SEPIC, which are modified, including bidirectional SEPIC, coupled SEPIC, Interleaved SEPIC, etc., have much better performance, ranging from 94% to 98% making the topology the best contender to be used for EV Charging applications. Bidirectional SEPIC topology was found to be ideal for on-board EV charging applications, whereas if the application is off-board EV Charging, then in that case, Interleaved or Coupled Inductor topology was found to be appropriate.

The study on steady state analysis of the topologies and hence the performance comparison helped in the identification of an appropriate SEPIC topology with reference to critical parameters. In comparison with the prior works, SEPIC variants like interleaved, bidirectional, or even coupled inductor topologies provide better performance in terms of switching losses reduction, efficiency improvement, and voltage ratio improvement.

Reference [4] explains the implementation of the state-of-the-art SEPIC Converter, whose efficiency is maximized by only up to 88%, with significant losses of around 20 W. In contrast, the suggested converters provide much better performance in terms of all the critical parameters, making them an ideal contender for charging electric vehicles. As far as the interleaved configuration is concerned, reference [15] represents an interleaved configuration, which was a 3-phase SEPIC variant; however, upon simulation, it was found that the efficiency can be maximized to 96 to 99% with reduced switching losses with interleaving, quasi-resonant switching, and isolation techniques. Robustness of the system simulated was seen with the voltage ratio attainment of around 1.9 pu compared to [15].

6.1. Future Research

Future investigations must primarily focus on enhancing SEPIC topology to attain much higher efficiency, improve power density, and reduce related losses. This objective can be attained with the introduction of advanced techniques like soft switching and the incorporation of semiconductor substances like SiC or GaNi. Further research on control strategies, Fuzzy logic, predictive control, based algorithms, etc., can be adopted under various dynamic load conditions. In addition to all of this, experimental implementation of the SEPIC topology with renewable systems or even exploration of smart grid infrastructure for integrating SEPIC Topology can be incorporated to assess the long-term reliability and efficiency tracking in real-world scenarios.

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