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Original Article

Novel XOR-XNOR Logic Gate: A Paradigm of Low Power Consumption and Energy Efficiency

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Abstract *- This study takes a close look at the numerous XOR and XNOR cell designs that have been reported throughout the years, beginning with the earliest ones and working all the way up to the most current ones that have been published. The study then proposed five new XOR structures and two new XNOR designs, with potential applications in error detection, logic comparators, cryptographic algorithms, and other fields, while comparing their performance to that of existing designs from other researchers pertaining to latency, power lag solution, and dissipation of power. During the course of this investigation, technical files pertaining to both 32nm and 16nm processing will be utilized. The voltage of the power supply is going to be 0.6v. A thorough comparison of proposed XOR and XNOR gates with existing XOR-XNOR gate designs at the level of the transistor relying on input voltage levels, average current propagation latency, energy efficiency of the proposed circuit transistor counts, and amount of power usage has been carried out. A thorough evaluation unambiguously reveals that the proposed designs outperform their equivalents in terms of power consumption, latency, area efficacy, and total energy efficiency. The Synopsys HSPICE tool is employed to simulate the suggested circuits.*

Keywords *- Digital circuits, Full adder, Power-delay product, Propagation delay, Transistor count.*

1. Introduction

The all-pervading electronic systems that are present in our lives today are now an integral component of our regular routine. Evidence obtained by the adoption of cell phones, smart cards, and other electronic gadgets clearly indicates the growth of the semiconductor sector in the last few years. Portability is the major design issue for IC engineers, which compels them to make devices with low power dissipation but without compromising their performance. Microprocessors, digital communication devices, and digital signal processors all make up a sizeable component of the digital circuits found in electronic systems. With the increase in integration levels, the feasibility of a circuit gets limited by rising power dissipation and space utilisation [1]. To accomplish the reduction in circuit size and amount of dissipation in the power of these systems while maintaining their speed, designers are working to meet the increasing need for and popularity of devices that are powered by batteries, like smartphones, tablets, and laptops. As dynamic and static components of power become more and more entwined, power is now viewed in relation to area and speed. The optimization that was done to increase speed had undesirable impacts on the amount of power used. Because power optimization has a negative impact on circuit performance, it is clear that circuits cannot operate at high frequencies while consuming little power, and vice versa. Due to the high-speed computing and sophisticated functionality needed by portable and handheld devices, low-power solutions are necessary. When it comes to applications of this nature, the average amount of power that must be consumed is a very significant design constraint to take into consideration. To optimise power and adhere to power limits, multiple iterations must be made. On all levels of abstraction, optimization is being done to cut down on energy usage. Optimising at the beginning of the design process has a significant impact on the outcome. With the reduction in size of the device, the amount of power lost due to leakage rose exponentially and became a major worry. Subthreshold leakage currents are increased as a result of shorter channel lengths, which occur as a direct result of a reduction in the overall size of the devices. Transistors have a limited ability to turn off due to this current. Because of the conditions that have been mentioned, minimising the amount of power that is lost due to leakage should be one of the primary focuses of a designer who is working on improving the power efficiency of VLSI circuits. In every system, there is a predetermined cap on the amount of power that may be used, and it is vital to select techniques and circuits that can keep up with the required amount of power [2].

Many different kinds of integrated circuits, including arithmetic and encryption circuits, make extensive use of the exclusive-OR (XOR) logic gate [3]. This fact is particularly true for devices that are used to carry out arithmetic operations, which include complete adders [4][5], magnitude checkers, parity detectors, and error-detection and correction modules. The XOR gate is an essential component of virtually all digital circuits, but it is notably important to the vast majority of encryption protocols. XOR Encryption is a method of data encryption that is difficult to break using a swinish-effort method, which involves producing arbitrary encryption keys in an attempt to associate them with the proper one. This encryption method is used to protect sensitive information [6].

The correct moniker for the Exclusive OR gate is "XOR." Whenever one of the XOR gate's inputs is only 1, it indicates that the outcome is 1. It is put to use for the purpose of encrypting the binary numbers. It conducts input modulo addition without carrying over. For this reason, the XOR gate is sometimes referred to as an equality detector and an inequality detector. The XOR gate's functionality can perhaps be implemented in a multitude of ways depending on the context. Only in the event that a single entry value is 1, Exclusive-OR gate creates output value 1 as a result. Instances in cases where the count of input highs is odd only result in a high output from the XOR gate. In the case of two inputs with differing logic levels, the XOR gate's output becomes high [7] [8]. Using a truth table as a guide, Table 1 clarifies the basic workings of the Exclusive-OR gate. A vital attribute of the EX-OR gate is the “controlled inverter”. Take into consideration the XOR gate, which has A and B as inputs and outputs Y. Let us examine the instance when one of the XOR gates two inputs, denoted by the letter A, is always set to the logic 1 value. In this scenario, result Y of the EX-OR circuit is always identical to the complemented value of the input B. On the other hand, when input A is always set to the logic 0 level, the result line Y is always an uncomplemented level of the incoming signal B. In short, when A=1; Y= $\overline{B}$ and A=0; Y= B.

There are many design styles employed by researchers over the years for constructing XOR and XNOR logic designs. CMOS design style, Pass transistor design style, transmission gate-based structure, Gate diffusion input technique, hybrid design style, and others. The main issue while using PTL, i.e. Pass Transistor logic, is that the NMOS substrate is not connected with the ground, which causes it to have a body effect; also, NMOS passes weak '1'. NMOS-PTL is a strong '0' passing device. In the case of PMOS PTL, it is a strong'1' passing device, so it is not possible to obtain full swing output, which causes malfunctioning of the equipment, which requires utmost precision. Though a Pass Transistor Logic (PTL) can make the circuit with a reduced number of transistors, its performance can be compromised as it has a threshold voltage drop issue.

Table 1. Truth Table of XOR-XNOR Gate

A	B	A XOR B	A XNOR B
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

So many researchers approach toward transmission gate design style, which is the parallel combination of NMOS and PMOS. It acts as a bidirectional switch, which overcomes the shortcomings of NMOS and PMOs. It has a control signal, which has a hold over the output result. It gives full swing output waveform. However, it has an issue when connected in cascaded form, as the longer distance from the power supply can distort driving capability. The gate-input technique is also widely used, but it is not possible to obtain full swing with it as it is based on the principle of pass transistor and CMOS inverter.

In this paper, a hybrid design style is incorporated along with a feedback loop to ensure of having full swing output, which can become beneficial further to be employed in many applications and able to give better results in comparison to existing designs. The structure of the paper can be seen in the following. In Section 2, previous work is evaluated, and specifics concerning the design of the circuits of the XOR-XNOR gates are assessed. In Section III, proposed Exclusive OR- Exclusive-NOR logic gate circuits are devised. The analysis and presentation of the simulation results is done in Section 4. The proposed ideas are compared to existing designs for evaluation and validation. The article is brought to a close with Section 5.

2. Previous Work

N. Zhuang [5] designed the XOR cell with only 6 transistors based on the transmission gate theory demonstrated in Figure 1. The Presented design utilized a combination of inverters and a transmission gate. In the case of A=1, the result line of the circuit is the inverse of B. Then strong ‘1’ AB’ signal is obtained. Whenever A is set to "LOW," then signal B will be sent unaltered and in full to the output terminal. As a result, the output will have an acceptable A'B signal level. Figure 1 shows the XOR gate design based on transmission gate theory [5]. In accordance with [7], the DPTL design was used to create the Full Swing XOR/XNOR circuit.

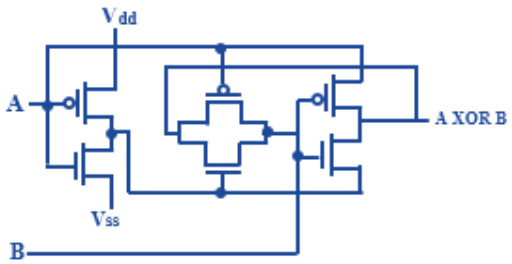

Fig. 1 XOR Circuit Proposed by N. Zhuang [5]

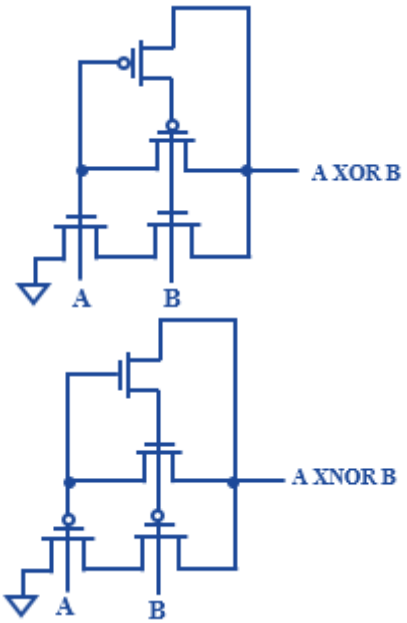

Fig. 2 XOR-XNOR Circuit Proposed by W. Jyh-Ming [7]

W. Jyh-Ming [7] has developed a concept for the XOR-XNOR logic gate, as displayed in Figure 2. In the event that the input signal AB equals 01, 10, 11, the waveform of the output gives full swing. Each PMOS will be active when AB = 00, and the output will provide a subpar "LO" signal. It means that in the instance of incoming signals AB getting low, the output end will show threshold potential higher than “LO” but can drive in two directions due to two PMOSs being ON. When functioning as an XNOR gate, the output is considered to be in full swing when the input combinations are written as AB = 00, 01, 10. During the time that AB is equal to 11, each NMOS will be active and will provide the low "HI" at the output end.

A. M. Shams [8] designed the circuit with six transistors, as displayed above in Figure 3. It produces poor 'LOW' at the XNOR node at the point where AB is equivalent to high. Insufficient voltage levels prevent it from operating at its best. A.M Shams [9] also proposed another circuit, as revealed in Figure 4.

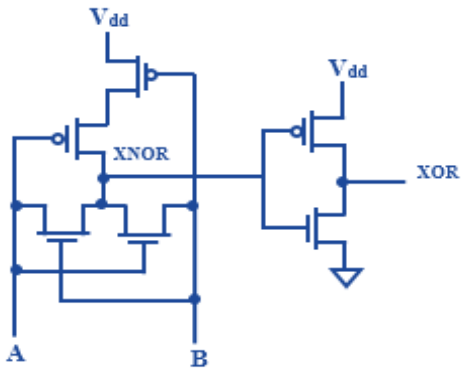

Fig. 3 XOR-XNOR Circuit Proposed by A.M.Shams [8]

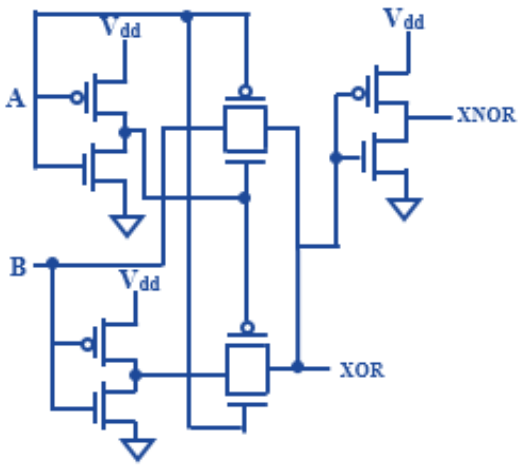

Fig. 4 XOR-XNOR Circuit Proposed by A.M.Shams [9]

However, despite its ability to function with a low voltage, it has a poor power efficiency rating. Because an inverter is utilised in this design to produce XOR and XNOR signals, the outputs of both of those logic gates exhibit significant time offsets. Author[9] suggested eight transistor circuit, illustrated in Figure 5; in the event that A & B both are high, the non-full swing result of the circuit, designated as XNOR, transmits weak logic "1," while XOR, designated as the output, transmits weak logic "0," respectively. Incompatible with very low voltage operations.

D. Radhakrishnan [10] postulated another six-transistor architecture of XOR and XNOR logic gates displayed in Figure 6, which eliminates the requirement on an inverter circuit. The utilisation of bidirectional PMOS and NMOS Transistors eliminates the transmission of weak logic, which exists in Figure 5. The XOR-XNOR logic gate shown in Figure 6 nevertheless manages to provide fully restored outputs at each of its nodes.

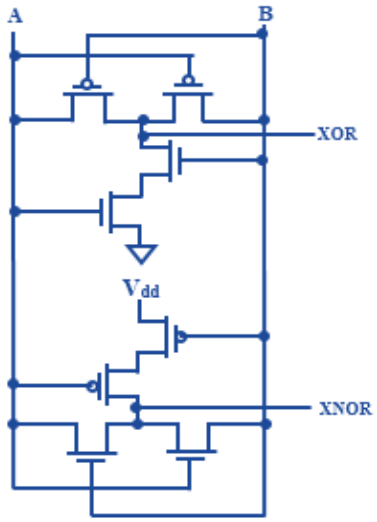

Fig. 5 XOR-XNOR Circuit Proposed [9]

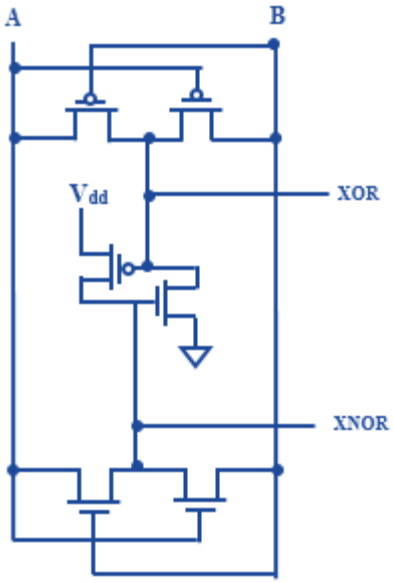

Fig. 6 XOR-XNOR Circuit Proposed by D. Radhakrishnan [10]

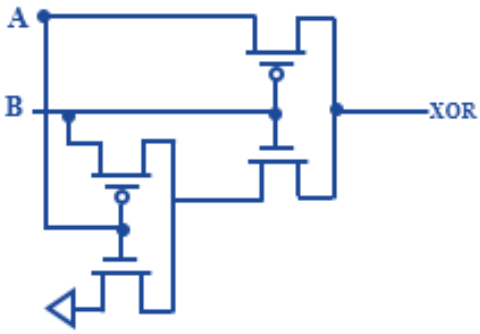

Fig. 7 XOR-XNOR Circuit Proposed by Hung Tien Bui [11]

Hung Tien Bui [11] is the one who came up with the idea of a powerless XOR gate that uses 4 transistors, as demonstrated in Figure 7, and does not require a power supply. It uses up to almost three times less power than the complementary CMOS solution could ever hope to. This design comprises a PTL-based multiplexer design. It is called powerless because none of the terminals of any transistor is connected to the power supply. The full-swing output waveform cannot be obtained through this circuit due to the presence of NMOS and PMOS-based PTL logic.The XNOR-XOR circuit that Mohamed Elgamel [12] developed was comprised of a combination of two PMOS and NMOS transistors connected in feedback connection. Figure 8 is expanded with a combination of back-to-back PMOS-NMOS transistors. This circuit consists of a total of 8 transistors as it is based on the principle of pass transistor logic. It gives a degraded output waveform. To overcome from this issue, the author used the back-to-back connection of PTL transistors. This solves the problem with the logic being too weak. It provides complete output in every respect. Low voltage operation is possible with this device.

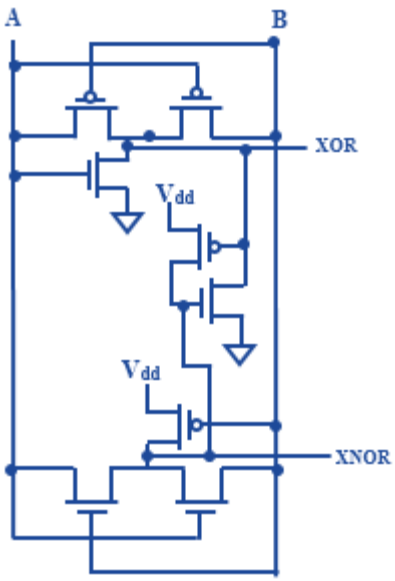

Fig. 8 XOR-XNOR Circuit Proposed by Mohamed Elgamel [12]

C.-H. Chang [13] came up with an innovative circuit design for the module that is not only capable of generating XOR and XNOR outputs concurrently mentioned in Figure 9 but also has the ability to do both at once. The XOR–XNOR circuit is enhanced by the addition of a PMOS-NMOS transistor connected in a feedback configuration. When the input pattern is "00" or "11," the previous circuit's problem with weak logic is resolved thanks to this new solution. The presence of a duo of successively linked PMOS transistors and NMOS transistors ensures complete oscillation of output throughout the input transformation to "00" and "11".

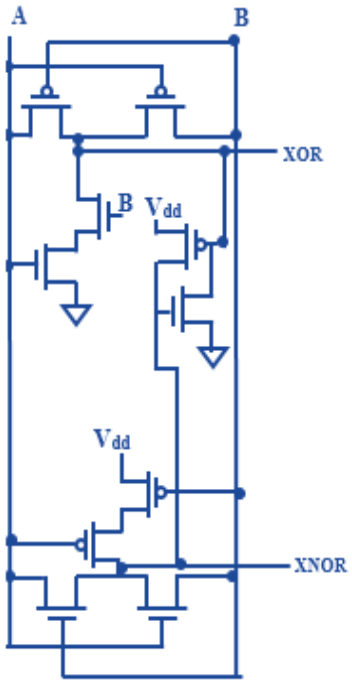

Fig. 9 XOR-XNOR Circuit Proposed by C.H Chang [13]

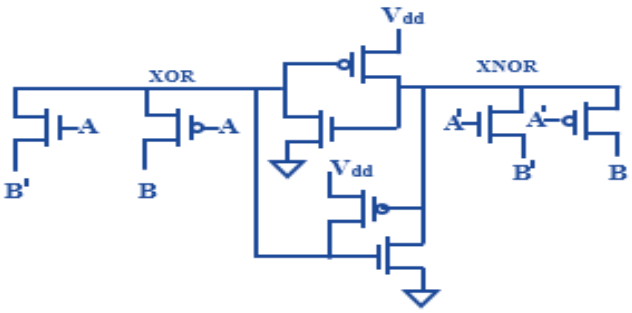

Fig. 10(a) XOR-XNOR Circuit Proposed by S.Goel [14]

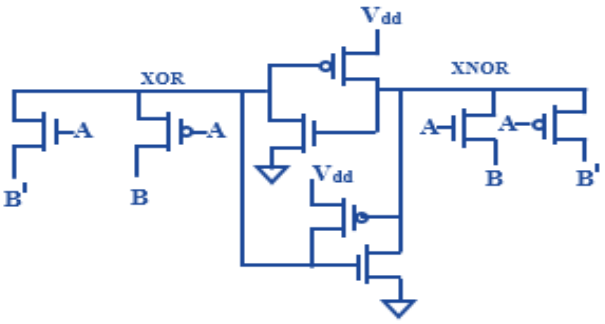

Fig. 10(b) XOR-XNOR Circuit Proposed by S.Goel [14]

Circuit topologies using double feedback were presented by S. Geol [14] in Figures 10(a) and 10(b), which require 12 and 10 devices, respectively. All provide lower power dissipation and improved noise immunity. S.Goel also postulated another fundamental structure, which is bolstered by four additional transistors: the combination of voltage level-up transistors and two pull-down transistors. To be more specific, the XOR function yields a "bad 1" when the input vector is "10." This is fixed by utilising the XOR network's two pull-up transistors, which are responsible for rectifying the issue.

In the same way, weak '0', which persists in the XNOR function, can be rectified by using two pull-down transistors. By utilising a feedback loop, the lingering two incorrect outputs are successfully repaired. The signal from the Exclusive-NOR output switches ON the feedback transistor, which results in a decrease in the XOR output to a "favourable low state" as a result of the action, which also switches ON the feedback transistor.

By doing so, the feedback loop is completed, and the logic level is set in motion. S.Goel also proposed another configuration, as displayed in Figures 11(a) and 11(b), in which it was discovered that the speed of the associated circuit may be increased by switching the reference inputs of the XNOR gate and also by connecting the gate connections of both transistors together. Due to the intrinsic slowness of PMOS transistors, passing an inverted signal through one causes an additional delay. The second set-up is known as "with reverse inputs."[16]

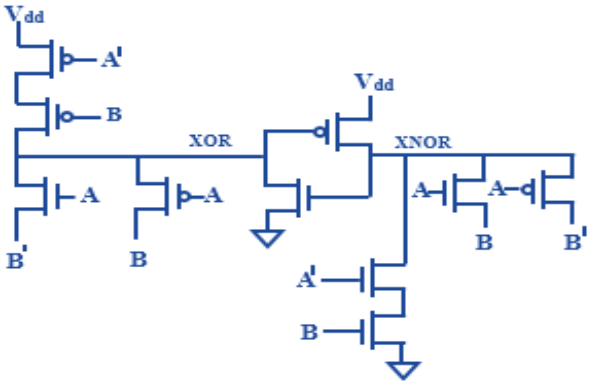

Fig. 11(a) XOR-XNOR Circuit Proposed by S.Goel [14]

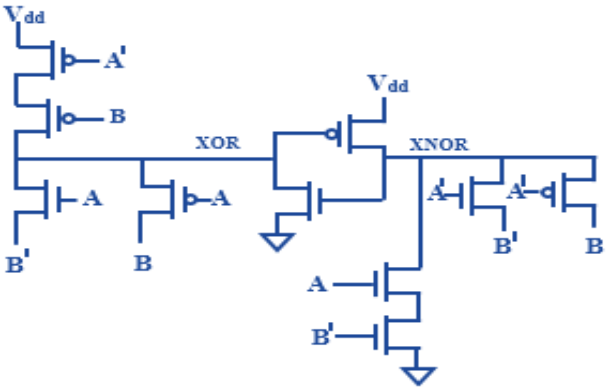

Fig. 11(b) XOR-XNOR Circuit Proposed by S.Goel [14]

R. Chowdhury [15] conceived an XOR gate that consisted of three transistors and featured an altered version of a Complementary-MOS, a complemented circuit, and a PMOS PTL, as pointed out in Figure 12. The adjacent inverter performs similarly to a typical CMOS inverter when input B is set to a logic high. Because of this, the value at the output Y is the opposite of the value of A. When the gate signal of incoming signal B is set to zero, the outcome of the CMOS inverter will have a high impedance. However, in the case where A = '1' and B = '0', a threshold voltage reduction along transistor M3 causes a voltage degeneration, and as a consequence, the output Y suffers a degradation in comparison to the source. By boosting the W/L ratio, it is possible to significantly reduce the voltage deterioration that is brought on by the threshold dip.

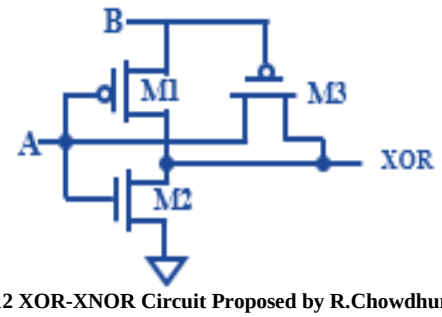

Fig. 12 XOR-XNOR Circuit Proposed by R.Chowdhury [15]

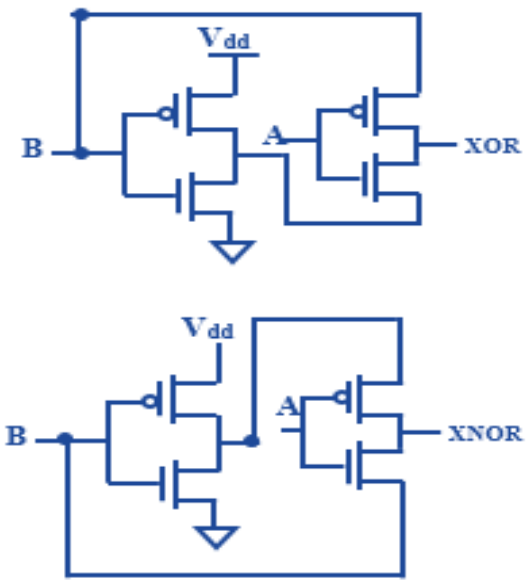

Fig. 13 XOR-XNOR Circuit Proposed by D.Wang [16]

D. Wang [16] introduced a design for an XOR and XNOR gate that uses four transistors and is focused on Gate-Diffusion-Input as depicted above in Figure 13. The main elements of the GDI cell comprise three input parameters: N (signal to the S and D of NMOS), P (signal to the S and D of PMOS), and G (common gate signal of N & P-type MOS. In contrast to inverters based on complementary metal oxide semiconductors, N and P types of transistors bulks are connected to N or P (respectively), allowing for arbitrary biasing.

CMOS inverters do not have this feature. Research on GDI is gaining momentum because of its alluring qualities that enable advancements in computational burden, number of gates, static energy losses, and signal oscillations in the VLSI sector. The GDI system has a flaw in that it requires a unique CMOS process, notably SOI or twin-tub CMOS; they are priced significantly higher than the common p-well CMOS. This limits the GDI system's ability to be used in many CMOS circuits.

Shiv Shankar [17] developed two different circuits of XOR-XNOR logic gates, which are depicted in Figures 14(a) and 14(b). The suggested designs are a modified form of a CMOS inverter and a PTL. While using the specified design I, the inverter circuit behaves normally close to a CMOS inverter whenever the value of B is set to one. As a result, the complement of input A is the result. The output, however, receives the very same logic value as input A because the PMOS pass transistor is turned ON. The design principle of this design is based on the CMOS inverter. Two level restorer transistors are also employed in it, which are deployed here to restore the output levels. The working of the whole device is, therefore, analogous to that of an XOR circuit with two inputs.

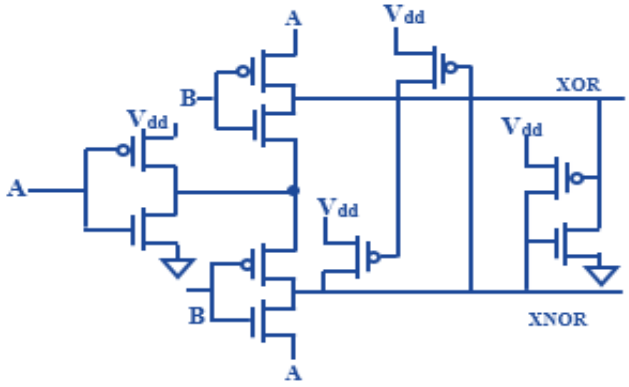

Fig. 14(a) XOR-XNOR Circuit-I Proposed by Shiv Shanker [17]

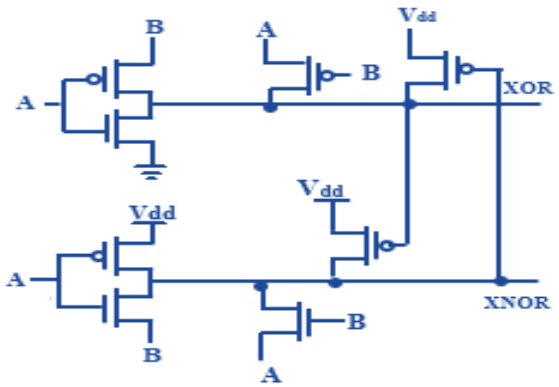

Fig. 14(b) XOR-XNOR Circuit-II Proposed by Shiv Shanker [17]

Nevertheless, it executes low oscillation input patterns, which causes the outputs that are associated with those patterns to be degraded by Vth. In the suggested method-II, shown in Figure 14(b), while B is at logic 1, PTL gets off, but the NMOS pass transistor gets off. As a result, the circuit's XOR and XNOR outputs have identical logic, with the XOR output being the complement of input A. When the logic level of input B is set to zero, the result of the circuit will be the opposite of 'A', and the XOR output will get an identical state as A. This is because the P-based PTL gets ON, while the N-based PTL will be OFF when the logic level of the input B is set to zero. This arrangement gets rid of a non-swinging action. For strong driving capability, the inverter circuit's aspect ratio must be high.

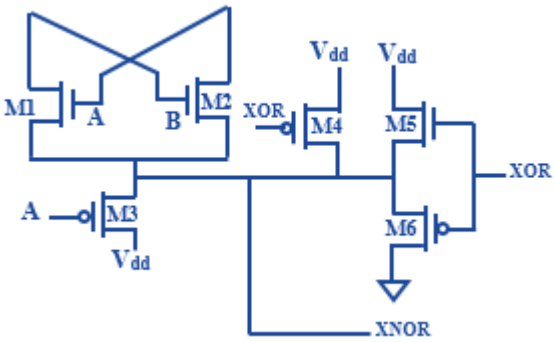

Fig. 15 XOR-XNOR Circuit Proposed by N.Ahmad [18]

N. Ahmad [18] came up with the idea of an XOR-XNOR logic gate that contains six transistors, as mentioned in Figure 15. It implements a concept known as a CMOS inverter in addition to a pass transistor. For the purpose of achieving a uniform output swing, M5 and M6 are employed as the generating result. To generate a reliable output of "1," transistors M3 and M4 are connected through a power supply. It is the job of transistor M4 to generate the output signal when the XOR logic gate produces a '0 in the case of input logic A=B=1. Under these circumstances, whenever M1 or M2 gets ON, it gives a faulty result of "1" in relation to the input of M5 and M6. The quality of the output will similarly deteriorate. As a means to produce a value that is acceptable for output, transistor M4 must be turned on when the XOR gate, which is connected to the output, is "0." This causes it to send the strong "1" through the power supply at an output terminal. R. Kumar [19] has presented a model for an XOR-XNOR gate that makes use of 5 transistors, which can be seen in Figure 16. It implements a concept known as a CMOS inverter in addition to a pass transistor. For the purpose of attaining a perfect output swing, the inverter circuit is used as a regulating output. As can be seen in Figure. 17, T. Sharma [20] described the XOR logic gate as having an architecture consisting of three transistors. There are two PMOS and one NMOS component in the mentioned design. In the case of '01' and '11', full-swing output will be obtained. Since the w/l of M2 is more than that of M3, the voltage at the Output connection depends on the functioning of the M2 transistor, and poor '1' will obtained when M2 and M3 get ON, which occurs due to input combination AB='10'. The reason for this is that when both M2 and M3 are turned on, their respective resistances will be brought into parallel. As a result, the whole resistance will decrease, which would lead to a reduction in output voltage. However, when AB=00, the threshold drop occurs over M2, making the output Y poorer than the input.

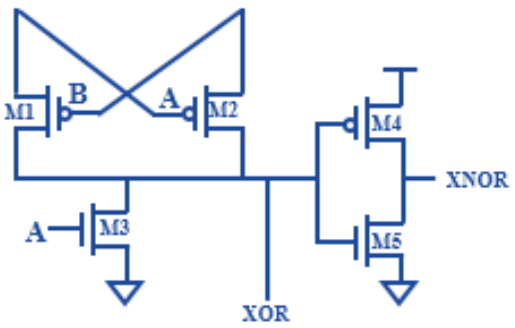

Fig. 16 XOR-XNOR Circuit Proposed by R.Kumar [19]

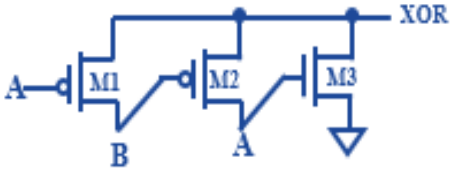

Fig. 17 XOR Circuit Proposed by T.Sharma [20]

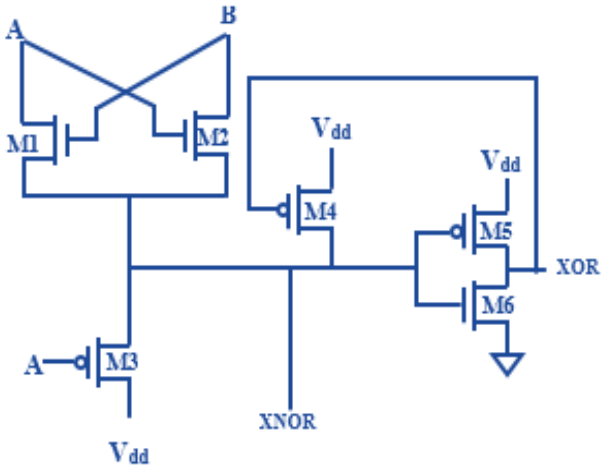

Fig. 18 XOR-XNOR Circuit Proposed by N.Ahmad [21]

N. Ahmad devised a low-power two-input XOR gate that uses 6T transistors, as presented in Figure 18 [21]. This gate permits low-supply operation with a tiny lagging. In order to realize a perfect output swing, the XOR circuit that has been presented uses a pass-transistor logic as its foundation and an inverter as its output controller.

Transistor M4 act as a level raiser, due to which the design of M1 & M2 should be selected such that it can maintain the voltage level at the XNOR node. Connections of Vdd are made towards the S terminal connection of M3 and M4 in order to yield a strong 1-signal. The transistors M1 and M2 are both active when A=B=1, which results in a feeble "1" signal being sent to the inverter's input. As a direct consequence of this, the quality of the output Y will likewise suffer.

Despite this, the feedback circuit ensures that transistor M4 is turned ON whenever Y equals 0. Therefore, the optimal level value "1" from the supply terminal is transmitted to the terminal of the receiving point of the inverter, which produces the complete signal "0" to be produced at Y. XNOR, on the other hand, produces a degraded '1' in response to the input pattern '11'.

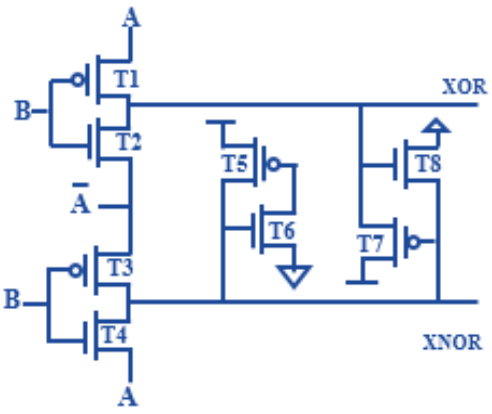

Fig. 19 XOR-XNOR Circuit Proposed by S.Musala [22]

S. Musala introduced an XOR/XNOR creation with 8 transistors [22], as depicted in Figure 19. The combination of transistors T5 and T6 in the regeneration loop is responsible for restoring the Bad '0' that was generated at Ex-OR. When inputs A and B are both logical zero, the transistors T2 and T4 turn on, causing XOR to produce a Weak One and Ex-NOR to produce a Good Zero. The restoration loop, which combines transistors T8 and T7, restores the produced weak "1" at Ex-OR. The inverted 'A' signal is obtained by using a Static CMOS inverter is used to produce a signal. For every possible input combination, it executes flawless full-swing actions.

S.Musala also created a total of eight different iterations, every one of which was based on distinct methodologies [23]; one structure is illustrated in Figures 20(a), 20(b), 20(c),20(d) and second approach is demonstrated in Figures 21(a), 21(b), 21(c) and 21(d)[23]. The first approach is based on the pass transistor concept, and the second approach is based on transmission gate topology along with static CMOS inverter to handle threshold voltage problems.The element count in pass transistor designs is typically lower, and they function with a minimal amount of power. The comparable design in the first framework assures high output signal voltage for all possible configurations. In every topology of Method-1, based on data A, just one PTL is active, as a consequence of which the matching value B is sent over to one of the output terminals.

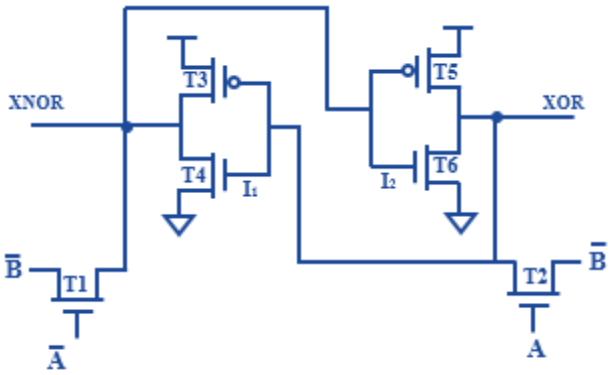

Fig. 20(a) PT based XOR-XNOR Circuit-1 by S.Musala [23]

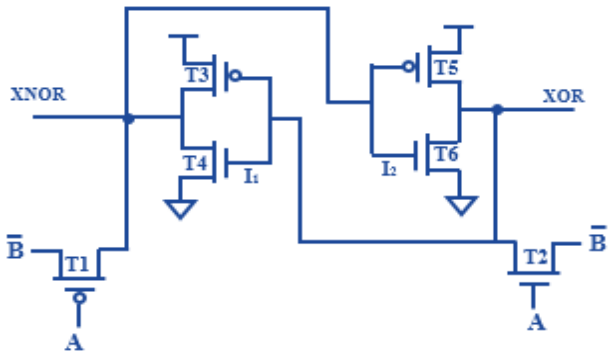

Fig. 20(b) PT based XOR-XNOR Circuit-2 by S.Musala [23]

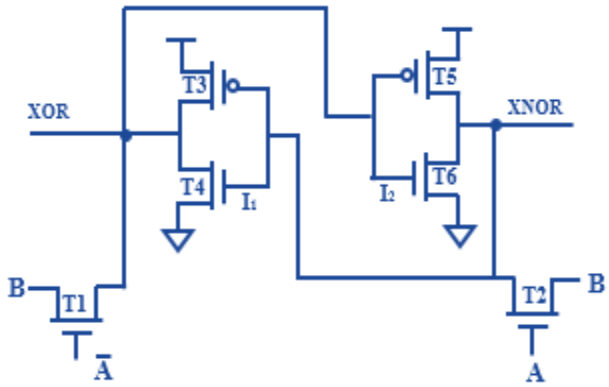

Fig. 20(c) PT based XOR-XNOR Circuit-3 by S.Musala [23]

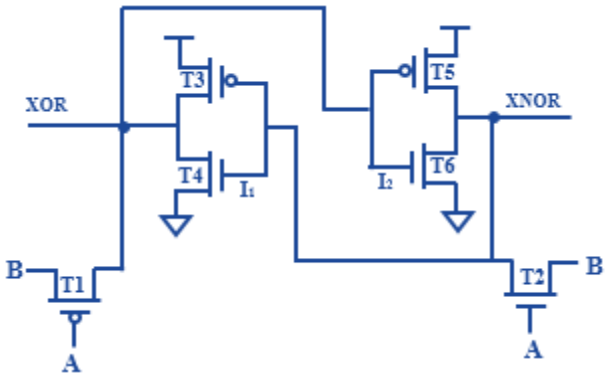

Fig. 20(d) PT based XOR-XNOR Circuit-4 by S.Musala [23]

This happens regardless of which input signal A is being processed (XOR or XNOR) [23]. The analogous output is then generated using a CMOS inverter, as shown in Figures 20(a) to (d). The proposed structure topologies of Design-2 for XOR/ XNOR logic are illustrated in Figures 21 (a), (b), (c), and (d), respectively [23]. Again, each version makes use of consecutively coupled static inverters, but instead of PTL, transmission gates are utilised in their place. In every design, on the basis of signal A, a single of the TGs will turn on at any one time, and the input signal that correlates to it, either B or B^{l}, will be inverted by a CMOS inverter before being routed to a specific output, either XOR or XNOR.

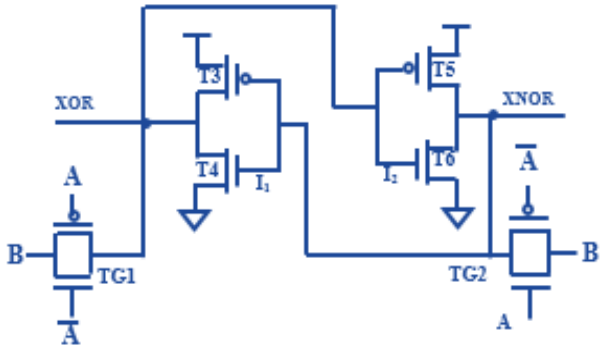

Fig. 21(a) TG based XOR-XNOR Circuit-1 by S.Musala [23]

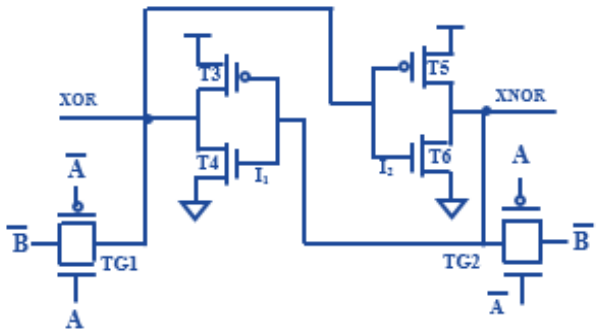

Fig. 21(b) TG based XOR-XNOR Circuit-2 by S.Musala [23]

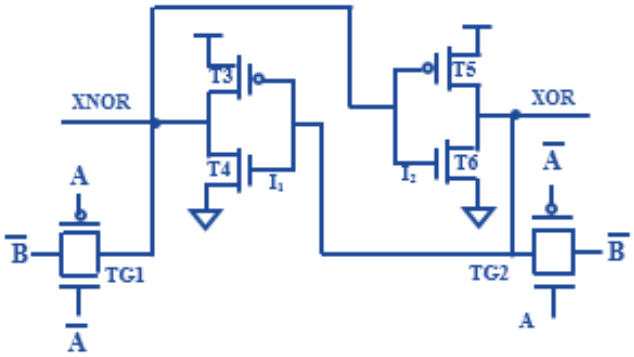

Fig. 21(c) TG based XOR-XNOR Circuit-3 by S.Musala [23]

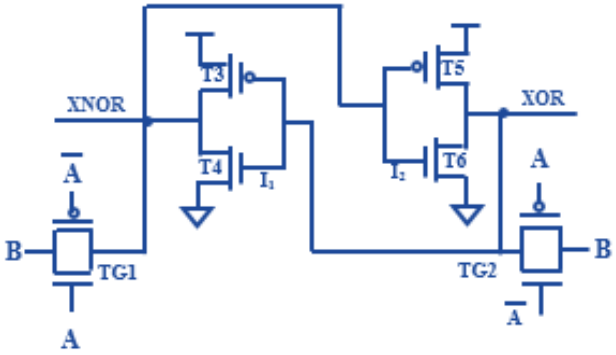

Fig. 21(d) TG based XOR-XNOR Circuit-4 by S.Musala [23]

The mirrored output is produced through the operation of the second CMOS inverter. Each possible input pattern is accommodated by the circuits with a full output swing. S. Harutyunyan [2] came up with an innovative design for an XOR gate that would consist of two PMOS and one NMOS coupled in the form of a diode, as shown in Figure 22.

Although this approach does not provide a complete output swing, it is possible to accomplish the desired result by including an output buffer in the circuit. The sources of these PMOS are coupled to input logic values A and B, and whenever two inputs are “zero," transistors M1 and M2 get switched ON. P-type MOS transistors send a weak "0" signal, and an NMOS transistor with such a diode connected will give a weak "0" signal to the output.

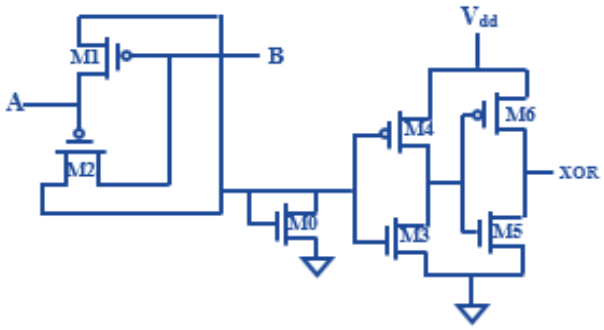

Fig. 22 XOR Circuit Proposed by S. Harutyunyan [2]

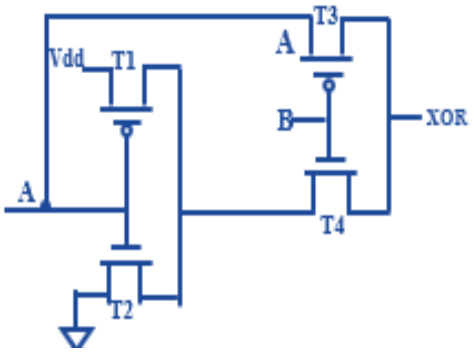

Fig. 23 XOR Circuit Proposed by H. Maity [24]

As a consequence of this fact, the output supply of the structure could not be able to drop lower than the threshold potential of that N-type Metal Oxide Semiconductor transistor. However, in some circumstances, that could lead to an output glitch. The logic value may collect false data if the threshold voltage of NMOS is high enough to reach the output inverter's changeover point. H. Maity [24] suggested utilising a 2:1 multiplexer, NOT gate, and four transistors to build a four-transistor, two-input XOR gate. The suggested 4T EXOR gate is seen in Figure 23, where the terminals A and B serve as inputs, and X is the destination point for the gate's output. The base of both the T1 and T2 transistors are linked to A via this connection. When the input is "0," the result is obtained from transistors T3 and T4, which are then turned on and off, respectively, causing X to equal A. As a result of T1 and T3 being OFF, as a result, T2 and T4 being ON when input B is '1', X equals A'.

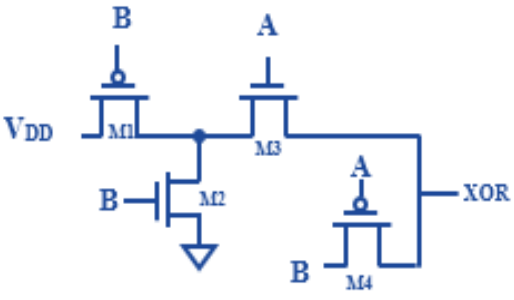

Fig. 24 XOR Proposed Design-I

Table 2. Transistor Status of Proposed design-I

Transistor	AB 00	AB 01	AB 10	AB 11
M1	ON	OFF	ON	OFF
M2	OFF	ON	OFF	ON
M3	OFF	OFF	ON	ON
M4	ON	ON	OFF	OFF
Output	**0**	**1**	**1**	**0**

3. Proposed Designs

Inside the presented manuscript, we have proposed five new frameworks of XOR logic gates and two new arrangements of XNOR logic gates, all of which are illustrated in Figures 24 to 30. Figure 24 depicts the XOR suggested circuit-I, which uses pass transistor logic as its foundation. This structure incorporates a total of four transistors into its design. If the input logic value of A and B is equal to '0', then the transistors M1 and M4 will become active, but the transistors M2 and M3 will remain inactive. Transistor M4 will switch on, passing the logic value of B to the intended output. Let us examine an additional scenario in which the input value A is equal to "1" and the input B is equal to "0." In this scenario, the logic gates M1 and M3 will be enabled, while the logic gates M2 and M4 will be inactive. Transistor M1 will then pass the logic value 1, which will then be passed via transistor M3, resulting in the logic value 1 being output from the XOR terminal. The status of transistors is mentioned in Table 2.

Figure 25 depicts the XOR suggested design-II, which makes use of one multiplexer circuit in addition to two pass transistors. This architecture makes use of a total of four transistors in its construction. The select line for the multiplexer is input signal B. It is common knowledge that PMOS transistors transmit a strong '1' signal while NMOS transistors transmit a strong '0' signal. As a consequence of the fact that transistor M1 M3 will be active for the input combination AB='00,' the multiplexer circuit will give the signal A at the output terminal. This is because transistors M2 and M4 will be inactive. In the event that the input logic signal AB is equal to the value '10,' the transistors M1 and M4 will become inactive, and the transistors M2 and M3 will become active as a result. As a consequence of this, the M3 transistor will send the logic value 1 to the output terminal. The same holds true for the combination when both AB='11,' in which case transistor M4 will provide logic 0 at the XOR terminal. With reference to AB='01,' transistors M2 and M4 will conflict with one another; hence, appropriate transistor scaling is required to resolve this issue. The corresponding status of transistors is stated in Table 3. In Figure 26, which is an expanded version of Figure 25, there is a discussion of a third potential design iteration for the XOR logic gate. One multiplexer circuit and one pass transistor are incorporated into this design, making 3T transistors in this configuration three.

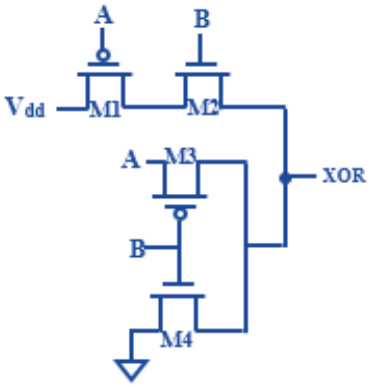

Fig. 25 XOR Proposed Design-II

Table 3. Transistor Status of XOR Proposed design-II

Transistor	AB 00	AB 01	AB 10	AB 11
M1	ON	ON	OFF	OFF
M2	OFF	ON	ON	ON
M3	ON	OFF	ON	OFF
M4	OFF	ON	OFF	ON
Output	**0**	**1**	**1**	**0**

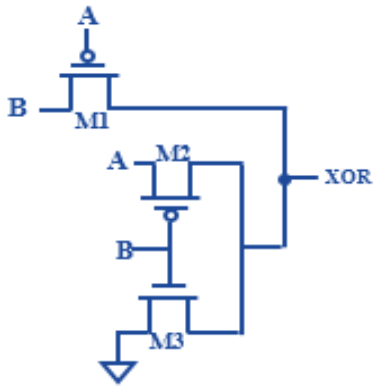

Fig. 26 XOR Proposed Design-III

In the event of input signal level AB being equal to '00,' transistors M1 and M2 will become active while transistor M3 will remain in its off state. As a result, the XOR output terminal will read '0' for both M1 and M2 transistors. Transistor M2 will become active and pass logic "1" gets available at the resulting terminal for the input combination AB="10," whereas transistors M1 and M3 will remain off. Likewise, when the input values are '11,' the transistors M1 and M2 will switch off, but the transistor M3 will become enabled and transfer logic '0' at the output port.

Nevertheless, if the input signal levels are A&B=01, then transistors M1 and M3 will be active, but transistor M2 will be off. In this instance, the PMOS transistor M1 requires the correct transistor sizing to provide acceptable result values. The information on correlating transistors can be found in Table 4.

Table 4. Transistor status of XOR proposed design-III

Transistor	AB 00	AB 01	AB 10	AB 11
M1	ON	ON	OFF	OFF
M2	ON	OFF	ON	OFF
M3	OFF	ON	OFF	ON
Output	**0**	**1**	**1**	**0**

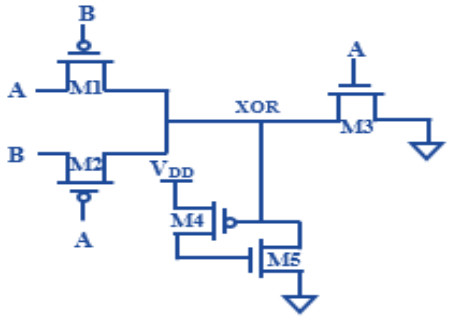

Fig. 27 XOR Proposed Design-IV

Table 5. Transistor status of XOR proposed design-IV

Transistor	AB 00	AB 01	AB 10	AB 11
M1	ON	OFF	ON	OFF
M2	ON	ON	OFF	OFF
M3	OFF	OFF	ON	ON
M4	ON	OFF	OFF	ON
M5	ON	OFF	OFF	ON
Output	**0**	**1**	**1**	**0**

Figure 27 depicts the fourth novel XOR gate design that uses feedback topology and pass transistor logic. It consists of a total of five transistors. PTL has a limitation that does not permit full-swing output, so the author introduced feedback transistors M4 and M5, which will guarantee complete zero at the output. As a result of the input application at their gate terminals, transistors M1 and M2 will turn ON for the input combination '00'. In reaction to this zero, transistor M4 becomes active, which in turn makes transistor M5 ON and makes a strong '0' at output. Table 5 lists the transistor's mode for the input combination "01, 10 & 11." A full swing output is delivered to the XOR terminal for input '10' with appropriate transistor size.

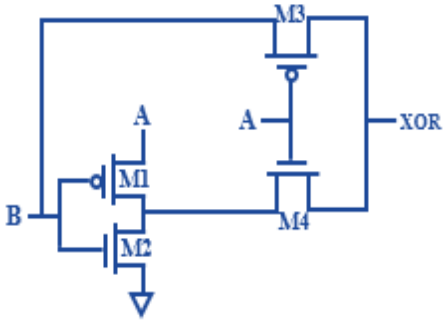

Fig. 28 XOR Proposed Design-V

Table 6. Transistor Status of XOR Proposed design-V

Transistor	AB 00	AB 01	AB 10	AB 11
M1	ON	OFF	ON	OFF
M2	OFF	ON	OFF	ON
M3	ON	ON	OFF	OFF
M4	OFF	OFF	ON	ON
Output	**0**	**1**	**1**	**0**

Further, the fifth structure of the XOR gate is exhibited in Figure 28, comprising a total of four transistors. It is based on the principle of the Gate diffusion input technique where the source of PMOS is connected to 'A' and the source terminal of NMOS is attached to the ground. A multiplexer design is also employed with the help of M3 and M4 transistors. M1 and M2 are GDI transistors. The drawback of this circuit is that it cannot give full swing for the input combinations '00' and '10' as M1 cannot pass strong '0' and M4 cannot pass strong '1' due to their properties. Their active and disabled state is mentioned in Table 6.

This article also includes two innovative designs of XNOR logic gates, which are shown in Figures 29 and 30. The suggested method-I of an EXNOR logic gate, depicted in Figure 29, is based on the PTL, feedback loop, and inverter-based idea. This design utilizes a total of 7T, designated as M1, M2, M3, M4, M5, M6 and M7. Transistors M1 and M2 are pass transistors that are based on PMOS, while transistors M3 are pass transistors based on NMOS. The feedback circuit comprises transistors M4 and M5, which will ensure complete zero. M6 and M7 transistors are responsible for obtaining XNOR output. When the input logic value is AB='00, transistors M1 and M2 become active, while transistors M3=OFF and M4 become active. As a result, transistors M1 and M2 pass the logic value "0," which is then passed through feedback transistors M4 and M5, which pull down the output to the logic '0' level. This signal value will pass through the inverter circuit, which results in XNOR output '1'. In the event that AB equals '01,' the transistors M1 get off while M2 becomes active; as a result, the value of 'B' will get inverted by transistors M6 and M7. Transistors M1, M3, and M4 will become abled for values AB=10, while M2 will be switched OFF.

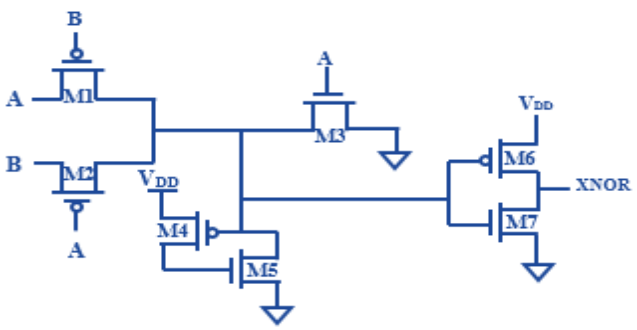

Fig. 29 XNOR Proposed Design-I

Table 7. Transistor Status of XNOR Proposed design-I

Transistor	AB 00	AB 01	AB 10	AB 11
M1	ON	OFF	ON	OFF
M2	ON	ON	OFF	OFF
M3	OFF	OFF	ON	ON
M4	ON	OFF	OFF	OFF
M5	ON	OFF	OFF	OFF
M6	ON	OFF	OFF	ON
M7	OFF	ON	ON	OFF
Output	**1**	**0**	**0**	**1**

In this situation, logic ‘0’ will arrive at the XNOR terminal. The final input combination, AB=11, will cause transistors M1, M2, M4, and M5 to become inoperable, while transistors M3 will become operational. Under these circumstances, transistor M6 will transmit the logic value "1" to the XNOR terminal. Table 7 outlines where respective transistors stand in terms of their ON/OFF states.

Figure 30 depicts the second proposed design of an XNOR logic gate based on an inverter and a multiplexer circuit. M1, M2, M3 and M4 transistors are used in this design. When AB='00,' transistors M1 and M3 are triggered, but transistors M2 and M4 are deactivated, causing transistor M3 to transmit binary '1' at the load port. In the event that the logic input values are '01', M1 and M4 will be enabled, but M2 & M3 get OFF.

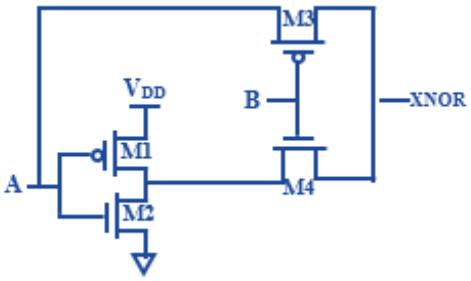

Fig. 30 XNOR Proposed Design-II

Table 8. Transistor status of XNOR proposed design-II

Transistor	AB 00	AB 01	AB 10	AB 11
M1	ON	ON	OFF	OFF
M2	OFF	OFF	ON	ON
M3	ON	OFF	ON	OFF
M4	OFF	ON	OFF	ON
Output	**1**	**0**	**0**	**1**

As a result, the output terminal will show a value of logic '0'. When the input logic signal AB="10," M1 and M4 will become inactive, but transistors M2 and M3 will become active, resulting in the appearance of the logic signal "0" at the XNOR output point. In the final instance, AB='11,' M1 and M3 will be turned off, while transistors M2 and M4 will be active, causing transistor M4 to send the logic'1' value to the output. Table 8 shows the state of the relevant transistors.

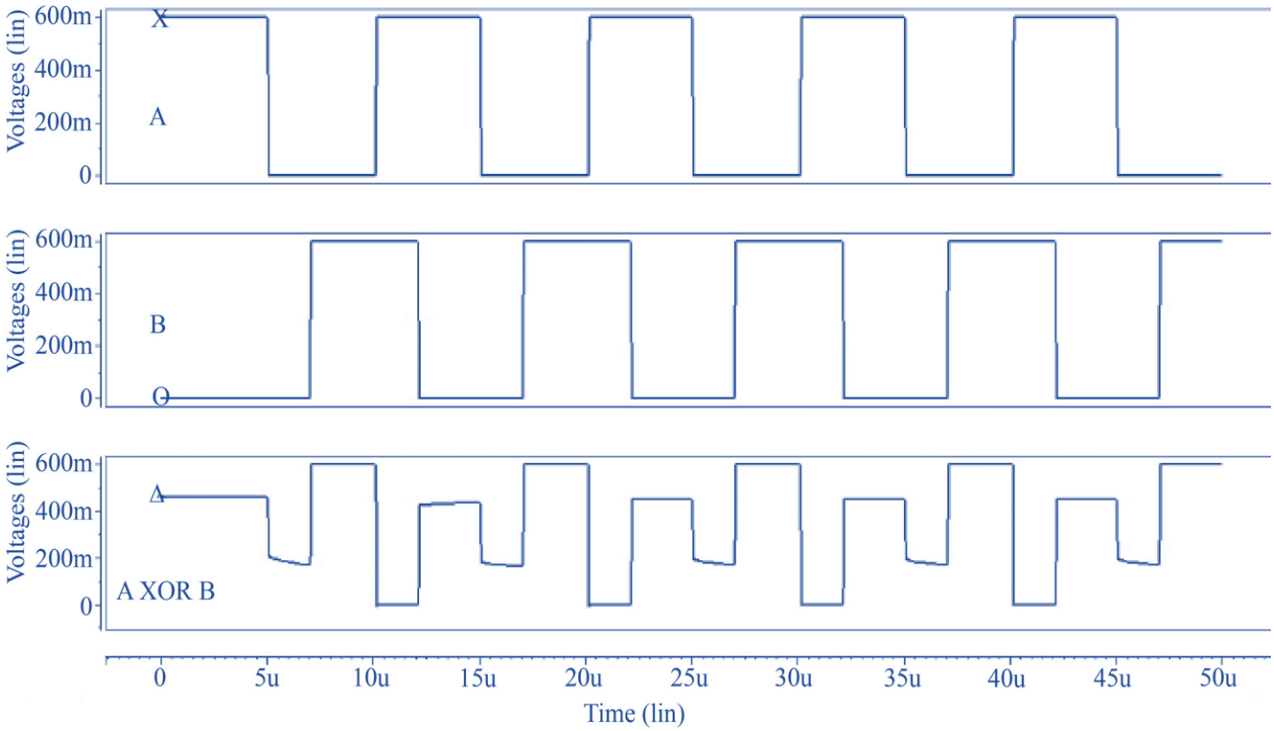

Fig. 31 Simulation waveform of XOR proposed design I

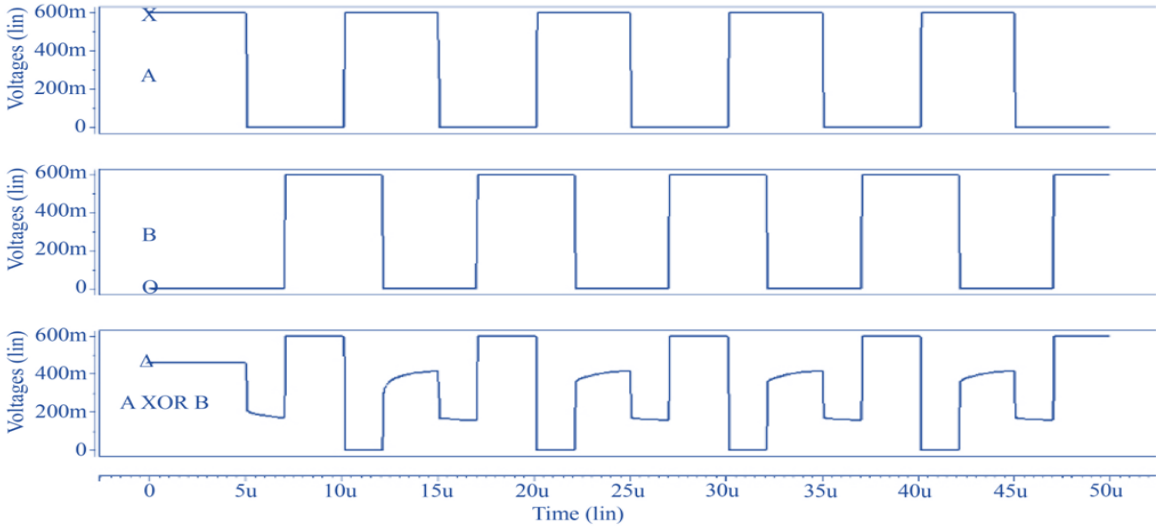

Fig. 32 Simulation waveform of XOR proposed design II

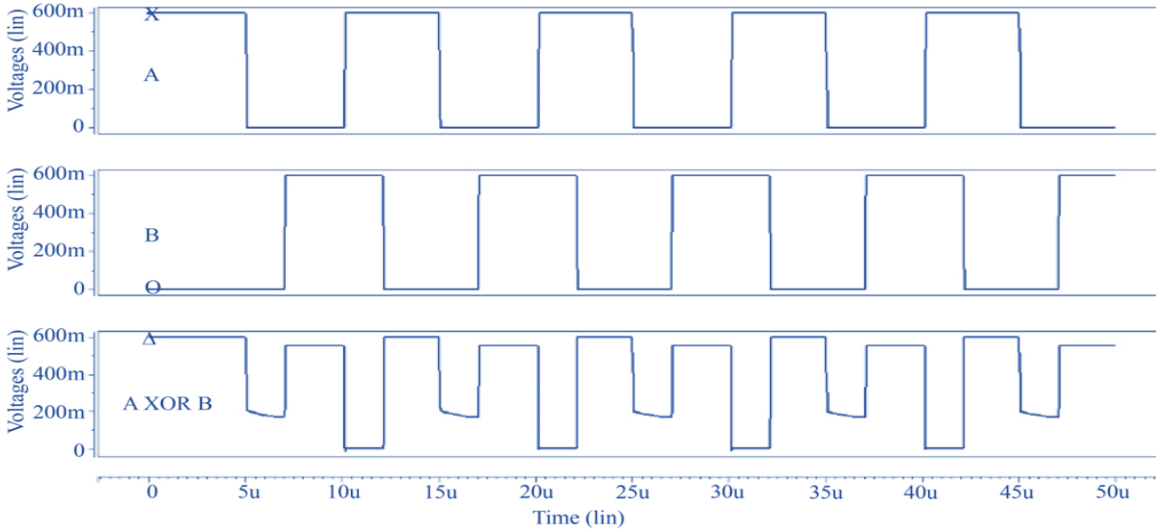

Fig. 33 Simulation waveform of XOR proposed design III

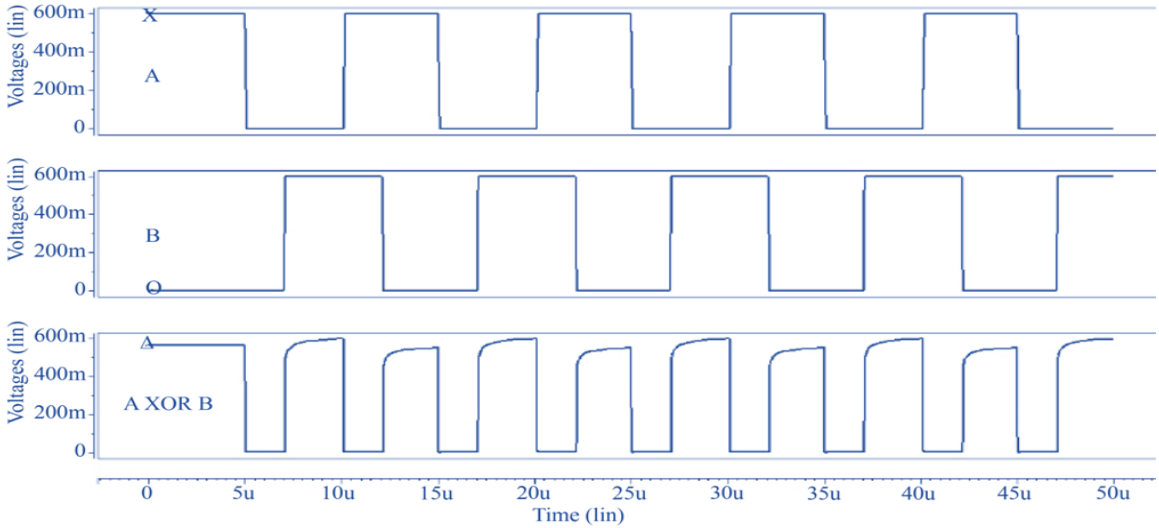

Fig. 34 Simulation waveform of XOR proposed design IV

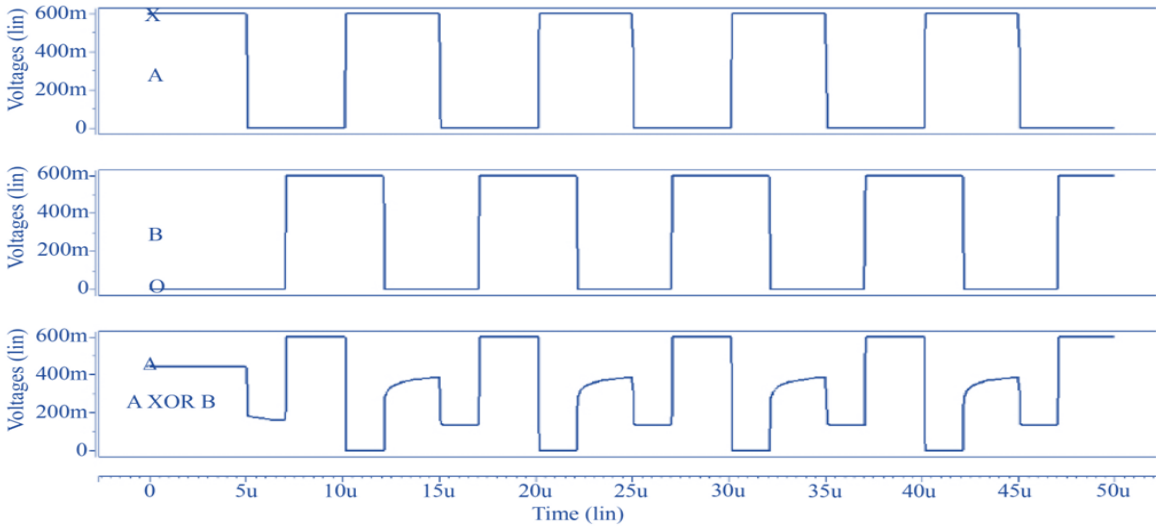

Fig. 35 Simulation waveform of XOR proposed design V

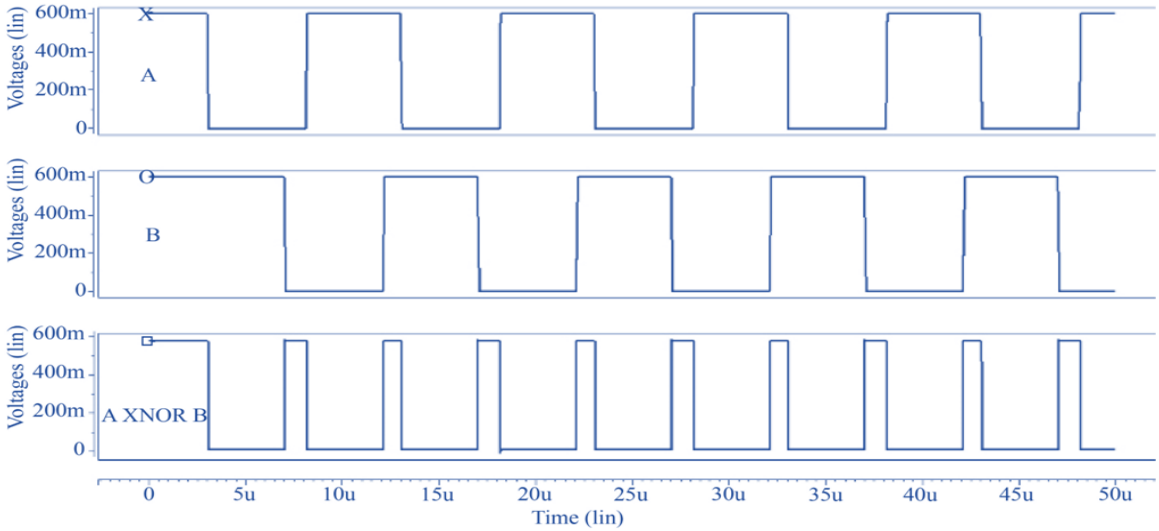

Fig. 36 Simulation waveform of XNOR proposed design I

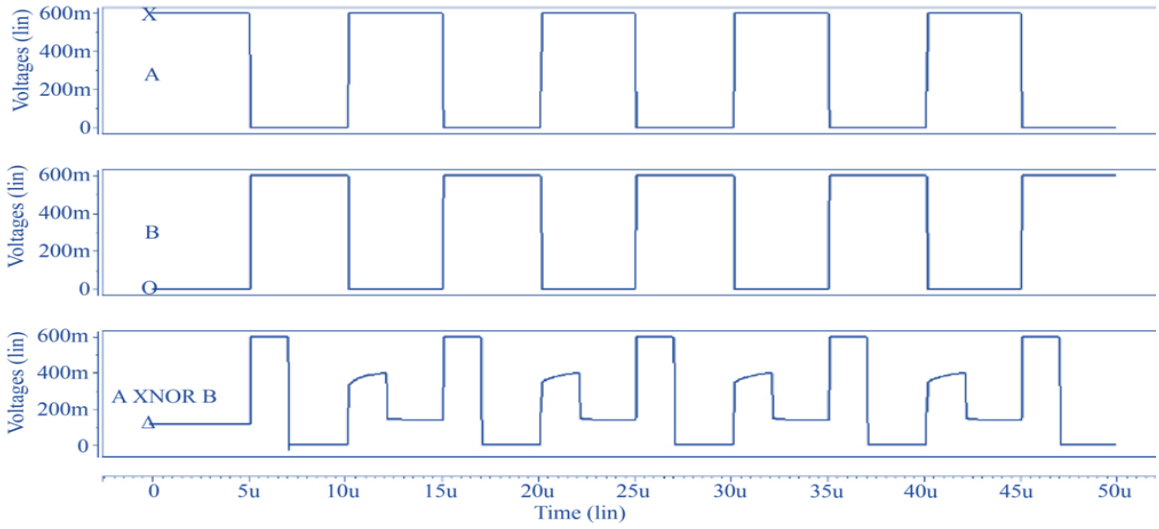

Fig. 37 Simulation waveform of XNOR proposed design II

Table 9. Comparative Analysis of Proposed XOR Designs and Other Structures in 32nm Technology at 0.6v power supply

Designs	Avg Power(w)	Delay(s)	PDP(J)
Fig 1 [5]	2.21E-12	2.67E-08	5.92E-20
Fig 2(a) [7]	1.28E-12	7.49E-08	9.58E-20
Fig 3 [8]	1.82E-11	2.95E-08	5.38E-19
Fig 4 [9]	3.56E-12	1.81E-08	6.44E-20
Fig 5 [9]	2.43E-12	3.84E-08	9.33E-20
Fig 6 [10]	2.73E-12	3.69E-08	1.01E-19
Fig 7 [11]	2.58E-12	8.37E-08	2.16E-19
Fig 8 [12]	2.76E-12	3.72E-08	1.02E-19
Fig 9 [13]	2.78E-12	3.74E-08	1.04E-19
Fig 10(a) [14]	3.56E-12	3.11E-08	1.11E-19
Fig 10(b) [14]	4.25E-12	3.69E-08	1.57E-19
Fig 11(a) [14]	4.40E-12	3.03E-08	1.33E-19
Fig 11(b) [14]	4.37E-12	3.23E-08	1.41E-19
Fig 12 [15]	1.96E-12	2.73E-08	5.35E-20
Fig 13(a) [16]	1.89E-12	2.87E-08	5.42E-20
Fig 14(a) [17]	3.31E-12	4.69E-08	1.55E-19
Fig 14(b) [17]	3.30E-12	2.67E-08	8.83E-20
Fig 16 [19]	1.75E-12	2.84E-08	4.97E-20
Fig 17 [20]	2.46E-12	2.67E-08	6.56E-20
Fig 19 [22]	3.65E-12	1.55E-07	5.66E-19
Fig 20(a) [23]	1.57E-09	1.99E-06	3.12E-15
Fig 20(b) [23]	1.59E-09	3.36E-08	5.34E-17
Fig 20(c) [23]	4.70E-10	3.20E-08	5.88E-18
Fig 20(d) [23]	4.70E-10	6.67E-08	3.13E-18
Fig 21(a) [23]	4.25E-12	4.68E-08	1.99E-19
Fig 21(b) [23]	4.12E-12	3.23E-08	1.33E-19
Fig 21(c) [23]	4.26E-12	2.38E-08	1.01E-19
Fig 21(d) [23]	4.25E-12	4.68E-08	1.99E-19
Fig 22 [2]	2.56E-12	2.79E-08	7.16E-20
Fig 23 [24]	2.19E-12	8.37E-08	9.96E-20
Fig 24 Proposed	1.18E-12	2.67E-08	3.15E-20
Fig 25 Proposed	1.18E-12	5.12E-08	6.04E-20
Fig 26 Proposed	1.11E-12	3.54E-08	3.93E-20
Fig 27 Proposed	3.16E-12	7.89E-08	2.49E-19
Fig 28 Proposed	1.77E-12	4.56E-08	8.07E-20

Table 10. EDP & Iaverage Analysis of Proposed XOR Designs and Other structures in 32nm technology at 0.6v power supply

Designs	EDP(J.s)	Iavg(amp)
Fig 1 [5]	1.58E-27	3.68E-12
Fig 2(a) [7]	7.18E-27	1.95E-12
Fig 3 [8]	1.59E-26	3.03E-11
Fig 4 [9]	1.17E-27	5.93E-12
Fig 5 [9]	3.58E-27	4.05E-12
Fig 6 [10]	3.72E-27	4.55E-12
Fig 7 [11]	1.81E-26	1.96E-12
Fig 8 [12]	3.79E-27	4.60E-12
Fig 9 [13]	3.88E-27	4.63E-12
Fig 10(a) [14]	3.45E-27	5.93E-12
Fig 10(b) [14]	5.79E-27	7.08E-12
Fig 11(a) [14]	4.02E-27	7.33E-12
Fig 11(b) [14]	4.55E-27	7.28E-12
Fig 12 [15]	1.46E-27	3.26E-12
Fig 13(a) [16]	1.56E-27	3.15E-12
Fig 14(a) [17]	7.26E-27	5.51E-12
Fig 14(b) [17]	2.36E-27	5.52E-12
Fig 16 [19]	1.41E-27	2.91E-12
Fig 17 [20]	1.75E-27	4.10E-12
Fig 19 [22]	8.77E-27	5.93E-12
Fig 20(a) [23]	6.20E-21	2.61E-09
Fig 20(b) [23]	1.79E-24	2.62E-09
Fig 20(c) [23]	4.05E-26	7.83E-10
Fig 20(d) [23]	2.09E-26	7.89E-10
Fig 21(a) [23]	9.31E-27	7.08E-12
Fig 21(b) [23]	4.29E-27	6.86E-12
Fig 21(c) [23]	2.40E-27	7.10E-12
Fig 21(d) [23]	9.31E-27	7.08E-12
Fig 22 [2]	2.00E-27	4.26E-12
Fig 23 [24]	8.34E-27	1.98E-12
Fig 24 Proposed	8.41E-28	1.96E-12
Fig 25 Proposed	3.09E-27	1.96E-12
Fig 26 Proposed	1.39E-27	1.85E-12
Fig 27 Proposed	1.97E-26	5.26E-12
Fig 28 Proposed	3.68E-27	2.95E-12

Table 11. Comparative Analysis of Proposed XOR Designs and Other Structures in 16nm technology at 0.6v power supply

Designs	Avg Power(w)	Delay(s)	PDP(J)
Fig 1 [5]	3.48E-12	3.12E-08	1.09E-19
Fig 2(a) [7]	2.10E-12	1.51E-07	3.18E-19
Fig 3 [8]	5.91E-12	3.86E-08	2.28E-19
Fig 4 [9]	5.17E-12	3.40E-08	1.76E-19
Fig 5 [9]	3.31E-12	3.33E-08	1.10E-19
Fig 6 [10]	3.98E-12	4.06E-08	1.62E-19
Fig 7 [11]	2.12E-12	2.04E-07	4.33E-19
Fig 8 [12]	4.06E-12	4.10E-08	1.66E-19
Fig 9 [13]	4.14E-12	4.03E-08	1.67E-19
Fig 10(a) [14]	5.55E-12	4.57E-08	2.54E-19
Fig 10(b) [14]	6.82E-12	4.37E-08	2.98E-19
Fig 11(a) [14]	7.40E-12	4.15E-08	3.07E-19
Fig 11(b) [14]	6.93E-12	4.61E-08	3.19E-19
Fig 12 [15]	2.13E-12	3.21E-08	6.84E-20
Fig 13(a) [16]	2.12E-12	2.89E-08	6.12E-20
Fig 14(a) [17]	5.41E-12	4.63E-08	2.50E-19
Fig 14(b) [17]	4.97E-12	3.56E-08	1.77E-19
Fig 16 [19]	2.93E-12	3.40E-08	9.95E-20
Fig 17 [20]	2.02E-12	3.28E-08	6.63E-20
Fig 19 [22]	5.76E-12	1.69E-07	9.74E-19
Fig 20(a) [23]	8.18E-10	5.25E-06	4.29E-15
Fig 20(b) [23]	1.41E-08	5.06E-06	7.14E-14
Fig 20(c) [23]	3.87E-11	2.09E-06	8.10E-17
Fig 20(d) [23]	3.83E-11	2.16E-08	8.26E-19
Fig 21(a) [23]	6.65E-12	5.19E-06	3.45E-17
Fig 21(b) [23]	6.23E-12	2.21E-07	1.37E-18
Fig 21(c) [23]	6.25E-12	2.22E-07	1.38E-18
Fig 21(d) [23]	2.97E-11	3.79E-08	1.13E-18
Fig 22 [2]	4.26E-12	5.16E-08	2.20E-19
Fig 23 [24]	2.14E-12	2.04E-07	4.33E-19
Fig 24 Proposed	2.12E-12	2.87E-08	6.07E-20
Fig 25 Proposed	2.23E-12	5.15E-08	1.15E-19
Fig 26 Proposed	2.04E-12	5.14E-08	1.05E-19
Fig 27 Proposed	4.23E-12	7.89E-08	3.34E-19
Fig 28 Proposed	2.02E-12	1.99E-07	4.01E-19

Table 12. EDP & Iaverage Analysis of Proposed XOR Designs and Other Structures in 16nm technology at 0.6v power supply

Designs	EDP(J.s)	Iavg(amp)
Fig 1 [5]	3.40E-27	5.80E-12
Fig 2(a) [7]	4.80E-26	3.50E-12
Fig 3 [8]	8.80E-27	9.85E-12
Fig 4 [9]	5.98E-27	8.62E-12
Fig 5 [9]	3.66E-27	5.52E-12
Fig 6 [10]	6.58E-27	6.63E-12
Fig 7 [11]	8.83E-26	3.53E-12
Fig 8 [12]	6.81E-27	6.77E-12
Fig 9 [13]	6.73E-27	6.90E-12
Fig 10(a) [14]	1.16E-26	9.25E-12
Fig 10(b) [14]	1.30E-26	1.14E-11
Fig 11(a) [14]	1.27E-26	1.23E-11
Fig 11(b) [14]	1.47E-26	1.16E-11
Fig 12 [15]	2.20E-27	3.55E-12
Fig 13(a) [16]	1.77E-27	3.53E-12
Fig 14(a) [17]	1.16E-26	9.02E-12
Fig 14(b) [17]	6.30E-27	8.28E-12
Fig 16 [19]	3.38E-27	4.88E-12
Fig 17 [20]	2.17E-27	3.37E-12
Fig 19 [22]	1.65E-25	9.60E-12
Fig 20(a) [23]	2.25E-20	1.36E-09
Fig 20(b) [23]	3.61E-19	2.35E-08
Fig 20(c) [23]	1.69E-22	6.45E-11
Fig 20(d) [23]	1.78E-26	6.38E-11
Fig 21(a) [23]	1.79E-22	1.11E-11
Fig 21(b) [23]	3.03E-25	1.04E-11
Fig 21(c) [23]	3.06E-25	1.04E-11
Fig 21(d) [23]	4.28E-26	4.95E-11
Fig 22 [2]	1.14E-26	7.10E-12
Fig 23 [24]	8.83E-26	3.57E-12
Fig 24 Proposed	1.74E-27	3.53E-12
Fig 25 Proposed	5.90E-27	3.72E-12
Fig 26 Proposed	5.40E-27	3.40E-12
Fig 27 Proposed	2.63E-26	7.05E-12
Fig 28 Proposed	7.98E-26	3.36E-12

4. Simulation Results

Using the Synopsys HSPICE tool, we run simulations at 0.6v on both 32 nm and 16 nm CMOS technology, simulating both the proposed and current XOR and XNOR circuits. Figure 31 depicts the transient behaviour of the XOR-suggested design-I that was discussed in Figure 24. The first two waveforms in this figure represent the inputs A and B, while the third waveform displays A XOR B. The performance analyses in terms of power dissipation, latency and power-delay-product, energy efficiency, and average current for each of the prospective designs, as well as XOR suggested design-I, are shown in Figures 38 to 42.

The simulated waveform of the XOR proposed design-II, III, IV, and V is depicted in Figures 32 to 35, respectively. The performance evaluation of the suggested XOR design is shown through bar graphs in Figures 38 to 42. It can be easily seen from the waveforms that the proposed Figure 29 gives perfect output. These graphs reflect the performance evaluation in terms of average power, latency, power-latency-product, average current, and energy efficacy. Another analysis in terms of energy efficiency and average current is demonstrated in Tables 10 and 12.

Similarly, the transient behavior of the XNOR-suggested designs I and II exhibited in Figures 29 and 30 is depicted in Figures 36 and 37. As per the result obtained, Figure 36 shows full swing output. The evaluation of the efficiency of the recommended XNOR methodology may be seen in the bar graphs that are located in Figures 43 to 47. These graphs illustrate the results of the performance assessment in terms of power, delay, PDP, energy capability, and average current.

5. Results and Discussion

Table 9 demonstrates the performance study of the supposed XOR logic gate in comparison to existing ones in 32nm technology with 0.6v supply voltage. The average power, the latency, and the propagation delay are utilized in the comparative analysis that is carried out. It is easy to see from the bar graph displayed in Figure 38 that the proposed XOR design-III, which is indicated in Figure 26, holds the smallest value in terms of average power when compared to other designs that are already in use. In order to analyze in clearway their performance analysis is provided by a bar graph in Figures 38, 39, 40, 41, and 42. In which it has been amply demonstrated that the power-lagging-product of the suggested XOR Framework I is the lowest of all.

Energy-delay products, i.e., EDP and average current analysis, are also carried out, which can easily be identified in Table 10. EDP is an important parameter in order to analyze the trade-off between energy efficiency and performance of design. It acts like the figure of merit; the lower the EDP, the better the energy efficiency of the circuit. From the table, it can easily be inferred that proposed design I of the XOR gate has the lowest EDP of all the prevailing existing designs.

Following the tradition of drawing the conclusion, it can be inferred that XOR proposed design III has the lowest average current among all the architectures, which makes it useful to apply in some power-consuming applications like multipliers, compressors, etc. Table 11 presents the results of a study that compared the newly proposed XOR logic gate to previously developed versions using 16 nm technology and 0.6 volts as the supply voltage. Based on the findings of this research, it is simple to deduce that the XOR proposed-V in Figure 28 circuit wastes less power than the ones that are already in use.

The proposed designs for the XOR gates I, II, III, and V have an extremely close level of similarity in terms of their average power. However, when compared to the other designs that are already in use, the power delay product of the XOR suggested design-I is the one that is the smallest. Once more, according to Table 12, it is evident that the proposed design-I of XOR is more energy efficient than previous designs. The average current is also analyzed here, which plays an important role in identifying the overall consumption, design, and sizing of the device. Based on the data in Table 12, it is evident that the XOR design shown in Figure 28 has the least average current.

Table 13 presents the results of a study that compared the proposed XNOR logic design-I and II to existing designs using 32 nm technology and 0.6 volts as the supply voltage. During the comparison study that is performed, the average power, the delay, and the propagation delay are all taken into consideration.

The chart presented in Figure 43 makes it very clear that the XNOR design-II that is being recommended, which is shown in Figure 30, has the lowest value in terms of the average power that it consumes when compared to the other designs that are currently being utilized. Figures 44, 45, 46, and 47 present a bar graph examination of their results in terms of delay, PDP, EDP and Iaverage, where it has been convincingly proved that the proposed XOR design-II has the minimum PDP of all.

Table 13 displays that the XNOR logic design recommended in Figure 30 boasts the least amount of power consumption in comparison to other existing designs. Average power analysis has numerous advantages, such as helping with battery life prediction in portable circuit design, as well as aiding in energy efficiency assessment, performance optimization, and thermal management. As per Table 14, suggested Figure 30 has the lowest energy-latency-product and minimal average current, making it applicable in various other fields.

Table 13. Comparative Analysis of Proposed XNOR Designs and Other Structures in 32nm Technology at 0.6v power supply

Designs	Avg Power(w)	Delay(s)	PDP(J)
Fig 2(b) [7]	1.96E-12	9.08E-08	1.78E-19
Fig 3 [8]	1.82E-11	2.12E-08	3.86E-19
Fig 4 [9]	3.56E-12	2.26E-08	8.05E-20
Fig 5 [9]	2.43E-12	1.31E-08	3.18E-20
Fig 6 [10]	2.73E-12	3.76E-08	1.03E-19
Fig 8 [12]	2.76E-12	3.81E-08	1.05E-19
Fig 9 [13]	2.78E-12	3.86E-08	1.07E-19
Fig 10(a) [14]	3.56E-12	3.05E-08	1.09E-19
Fig 10(b) [14]	4.25E-12	3.84E-08	1.63E-19
Fig 11(a) [14]	4.40E-12	2.92E-08	1.28E-19
Fig 11(b) [14]	4.37E-12	5.69E-08	2.49E-19
Fig 13(b) [16]	1.89E-12	7.03E-09	1.33E-20
Fig 14(a) [17]	3.31E-12	4.54E-08	1.50E-19
Fig 14(b) [17]	3.30E-12	5.14E-06	1.70E-17
Fig 16 [19]	1.75E-12	2.27E-08	3.97E-20
Fig 19 [22]	3.65E-12	5.72E-08	2.09E-19
Fig 20(a) [23]	1.57E-09	2.00E-06	3.14E-15
Fig 20(b) [23]	1.57E-09	6.67E-09	1.05E-17
Fig 20(c) [23]	4.70E-10	4.12E-08	1.94E-17
Fig 20(d) [23]	4.70E-10	1.70E-08	7.99E-18
Fig 21(a) [23]	4.25E-12	5.58E-08	2.37E-19
Fig 21(b) [23]	4.12E-12	2.23E-08	9.19E-20
Fig 21(c) [23]	4.26E-12	3.48E-08	1.48E-19
Fig 21(d) [23]	4.25E-12	5.58E-08	2.37E-19
Fig 22 [2]	2.56E-12	2.55E-08	6.53E-20
Fig 29 Proposed	3.43E-12	2.30E-08	7.89E-20
Fig 30 Proposed	1.63E-12	1.80E-08	2.93E-20

In a manner analogous, the suggested XNOR design-I and II are simulated in 16nm technology using 0.6v as the power source, and a comparative examination of these designs is carried out with regard to avg-power, delay, and power-lagging-product.

The findings of that investigation are summarised in Tables 15 and 16. It is easy to deduce, on the basis of the findings of this research, that the XNOR proposed-II circuit uses far less power than the ones that are currently being utilised.

Table 14. EDP & Iaverage Analysis of Proposed XNOR Designs and Other Structures in 32nm technology at 0.6v power supply

Designs	EDP(J.s)	Iavg(amp)
Fig 2(b) [7]	1.62E-26	3.27E-12
Fig 3 [8]	8.18E-27	3.03E-11
Fig 4 [9]	1.82E-27	5.93E-12
Fig 5 [9]	4.17E-28	4.05E-12
Fig 6 [10]	3.86E-27	4.55E-12
Fig 8 [12]	4.01E-27	4.60E-12
Fig 9 [13]	4.14E-27	4.63E-12
Fig 10(a) [14]	3.31E-27	5.93E-12
Fig 10(b) [14]	6.27E-27	7.08E-12
Fig 11(a) [14]	3.75E-27	7.33E-12
Fig 11(b) [14]	1.41E-26	7.28E-12
Fig 13(b) [16]	9.34E-29	3.15E-12
Fig 14(a) [17]	6.82E-27	5.52E-12
Fig 14(b) [17]	8.72E-23	5.50E-12
Fig 16 [19]	9.02E-28	2.92E-12
Fig 19 [22]	1.19E-26	6.08E-12
Fig 20(a) [23]	6.28E-21	2.62E-09
Fig 20(b) [23]	6.98E-26	2.62E-09
Fig 20(c) [23]	7.98E-25	7.83E-10
Fig 20(d) [23]	1.36E-25	7.83E-10
Fig 21(a) [23]	1.32E-26	7.08E-12
Fig 21(b) [23]	2.05E-27	6.87E-12
Fig 21(c) [23]	5.16E-27	7.10E-12
Fig 21(d) [23]	1.32E-26	7.08E-12
Fig 22 [2]	1.66E-27	4.27E-12
Fig 29 Proposed	1.81E-27	5.72E-12
Fig 30 Proposed	5.28E-28	2.72E-12

Both of the designs that have been presented for the XNOR gate, I and II, have a level of delay that is quite comparable to one another and are very close to being identical. Nevertheless, the power delay product of the XNOR recommended technique II is the one that is the lowest when compared to the other design features that are already in use. This is the case when compared to the other designs.

In addition to its role in estimating battery life for portable circuit design, average power analysis also assists in assessing energy efficiency, optimizing performance, and handling

thermal considerations when it comes to evaluating energy efficiency. It is evident from Table 15 that Figure 30, as suggested, exhibits the lowest energy-latency-product and minimal average current when compared to previous findings, making it applicable to a variety of fields that are not necessarily related to its primary application.It also boasts minimal power usage. The prevailing existing designs are mostly based on CMOS inverters and transmission gates, which increase the number of transistors and delay.

Also, as we know, while using transmission gate topology, an inverted signal of applied logic is also required, which contributes towards its area occupancy. The proposed designs depicted here are mostly based on pass transistors; to overcome their shortcomings, feedback topology is used. The use of PTL logic reduced the number of transistors, which in turn caused a decrease in power consumption. That is the reason the proposed design is able to achieve such results.

Table 15. Comparative Analysis of Proposed XNOR Designs and Other Structures in 16nm Technology at 0.6v power supply

Designs	Avg Power (w)	Delay (s)	PDP (J)
Fig 2(b) [7]	2.17E-12	1.45E-06	3.15E-18
Fig 3 [8]	2.14E-11	4.76E-08	1.02E-18
Fig 4 [9]	5.17E-12	4.19E-08	2.16E-19
Fig 5 [9]	3.31E-12	4.60E-08	1.52E-19
Fig 6 [10]	3.98E-12	3.76E-08	1.50E-19
Fig 8 [12]	4.06E-12	3.83E-08	1.56E-19
Fig 9 [13]	4.14E-12	3.83E-08	1.58E-19
Fig 10(a) [14]	5.55E-12	4.35E-08	2.42E-19
Fig 10(b) [14]	6.82E-12	4.98E-08	3.40E-19
Fig 11(a) [14]	7.40E-12	4.11E-08	3.04E-19
Fig 11(b) [14]	6.93E-12	4.56E-08	3.16E-19
Fig 13(b) [16]	2.63E-12	6.51E-08	1.71E-19
Fig 14(a) [17]	5.41E-12	4.04E-08	2.19E-19
Fig 14(b) [17]	4.97E-12	3.96E-08	1.97E-19
Fig 16 [19]	2.93E-10	4.17E-08	1.22E-19
Fig 19 [22]	5.76E-12	5.83E-08	3.36E-19
Fig 20(a) [23]	8.18E-10	4.17E-09	3.41E-18
Fig 20(b) [23]	1.41E-08	2.06E-06	2.91E-14
Fig 20(c) [23]	3.87E-11	1.33E-08	5.16E-19
Fig 20(d) [23]	3.83E-11	1.23E-08	4.71E-19
Fig 21(a) [23]	6.65E-12	5.16E-06	3.43E-17
Fig 21(b) [23]	6.23E-12	1.72E-07	1.07E-18
Fig 21(c) [23]	6.25E-12	1.83E-07	1.15E-18
Fig 21(d) [23]	2.97E-11	3.88E-08	1.15E-18
Fig 22 [2]	4.26E-12	4.52E-08	1.92E-19
Fig 29 Proposed	4.03E-12	4.32E-08	1.74E-19
Fig 30 Proposed	1.73E-12	5.28E-08	9.15E-20

Table 16. EDP & Iaverage Analysis of Proposed XNOR Designs and Other Structures in 16nm Technology at 0.6v power supply

Designs	EDP (J.s)	Iavg (amp)
Fig 2(b) [7]	4.57E-24	3.62E-12
Fig 3 [8]	4.85E-26	3.57E-11
Fig 4 [9]	9.05E-27	8.62E-12
Fig 5 [9]	7.00E-27	5.52E-12
Fig 6 [10]	5.64E-27	6.63E-12
Fig 8 [12]	5.97E-27	6.77E-12
Fig 9 [13]	6.05E-27	6.90E-12
Fig 10(a) [14]	1.05E-26	9.25E-12
Fig 10(b) [14]	1.69E-26	1.14E-11
Fig 11(a) [14]	1.25E-26	1.23E-11
Fig 11(b) [14]	1.44E-26	1.16E-11
Fig 13(b) [16]	1.11E-26	4.38E-12
Fig 14(a) [17]	8.85E-27	9.02E-12
Fig 14(b) [17]	7.80E-27	8.28E-12
Fig 16 [19]	5.09E-27	4.88E-10
Fig 19 [22]	1.96E-26	9.60E-12
Fig 20(a) [23]	1.42E-26	1.36E-09
Fig 20(b) [23]	5.99E-20	2.35E-08
Fig 20(c) [23]	6.86E-27	6.45E-11
Fig 20(d) [23]	5.79E-27	6.38E-11
Fig 21(a) [23]	1.77E-22	1.11E-11
Fig 21(b) [23]	1.84E-25	1.04E-11
Fig 21(c) [23]	2.10E-25	1.04E-11
Fig 21(d) [23]	4.46E-26	4.95E-11
Fig 22 [2]	8.68E-27	7.10E-12
Fig 29 Proposed	7.52E-27	6.72E-12
Fig 30 Proposed	4.83E-27	2.89E-12

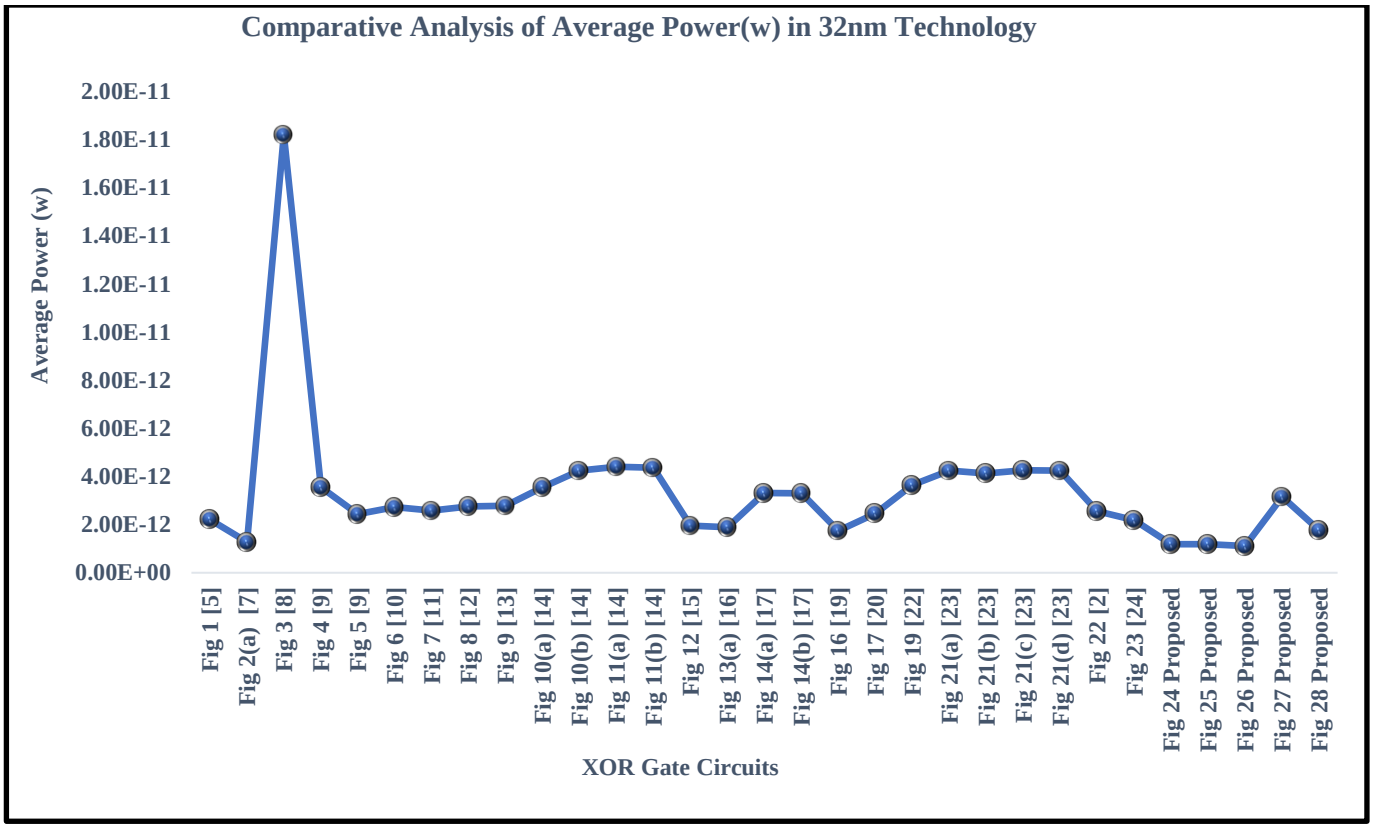

Fig. 38 Average Power Analysis of XOR Proposed design-I, II, III, IV and V with existing architectures

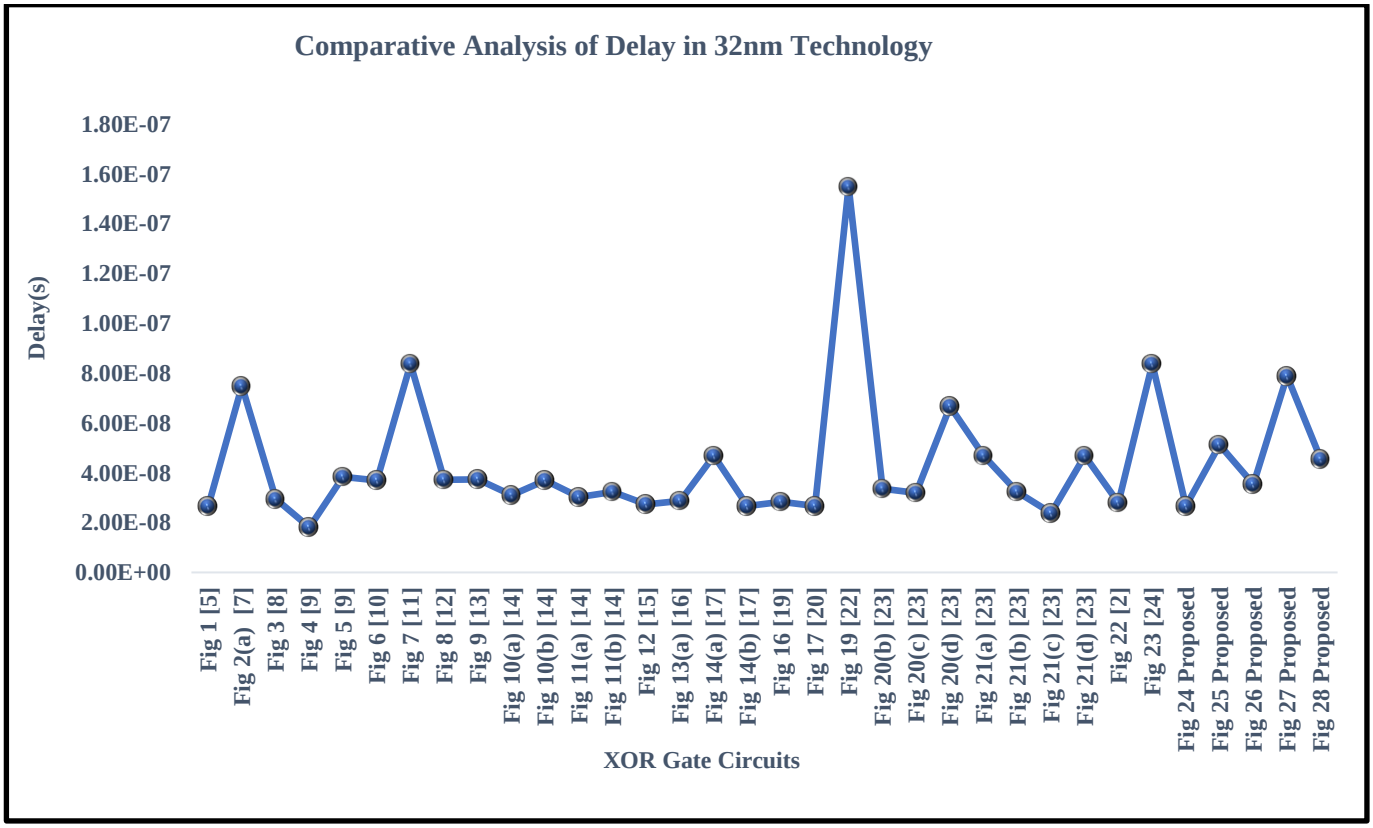

Fig. 39 Delay Analysis of XOR Proposed design--I, II, III, IV and V with existing architectures

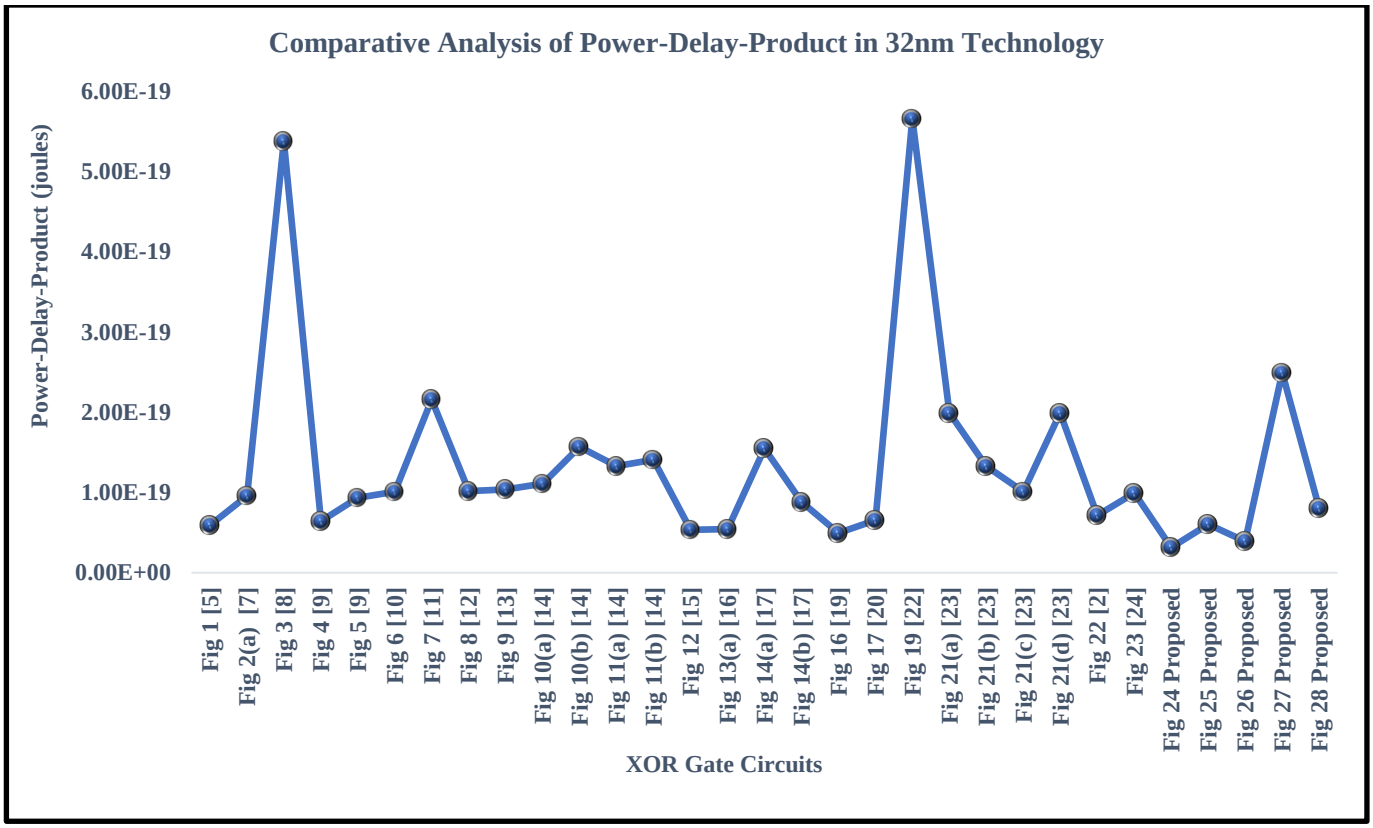

Fig. 40 Power-delay-product Analysis of XOR Proposed design- I, II, III, IV and V with existing architectures

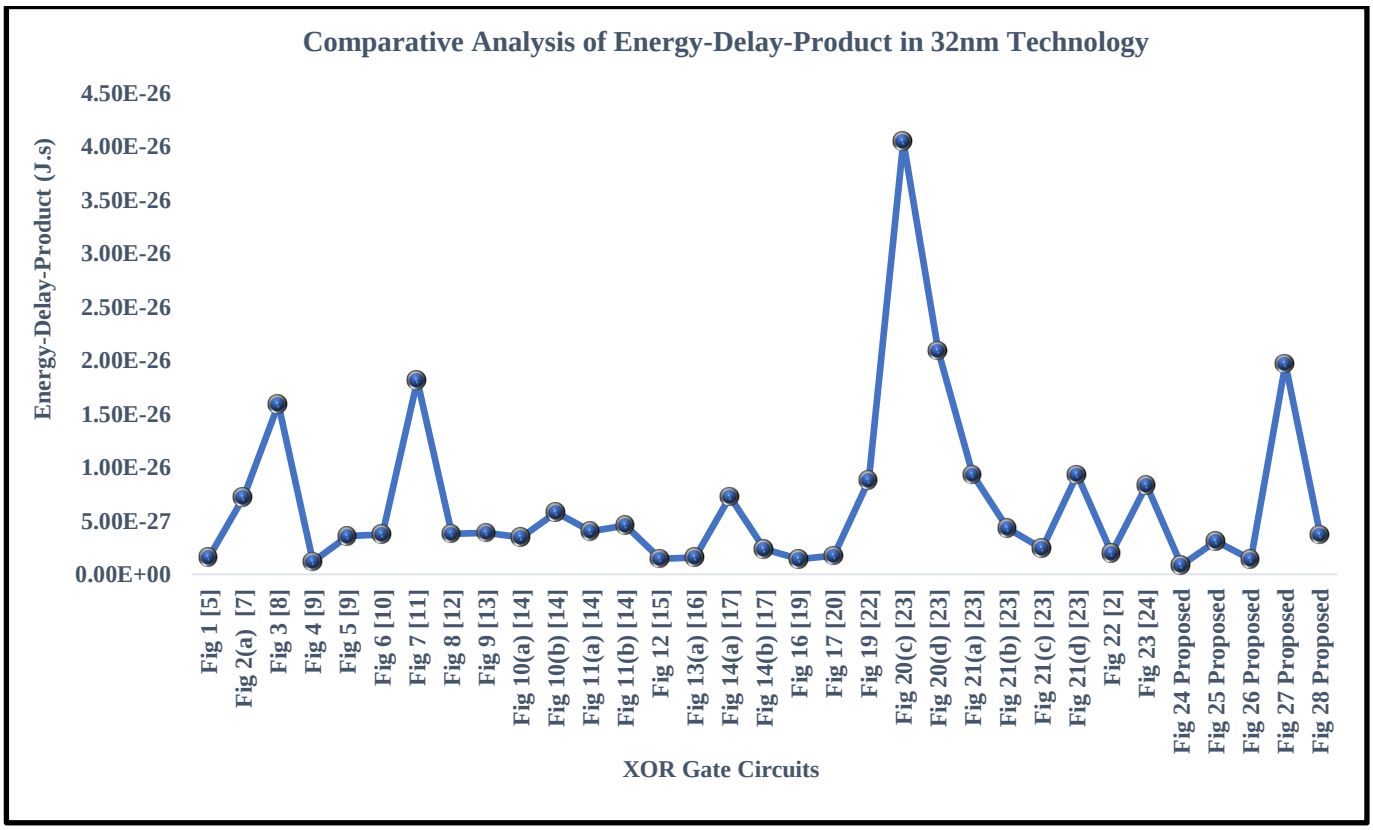

Fig. 41 Energy-delay-product Analysis of XOR Proposed design- I, II, III, IV and V with existing architectures

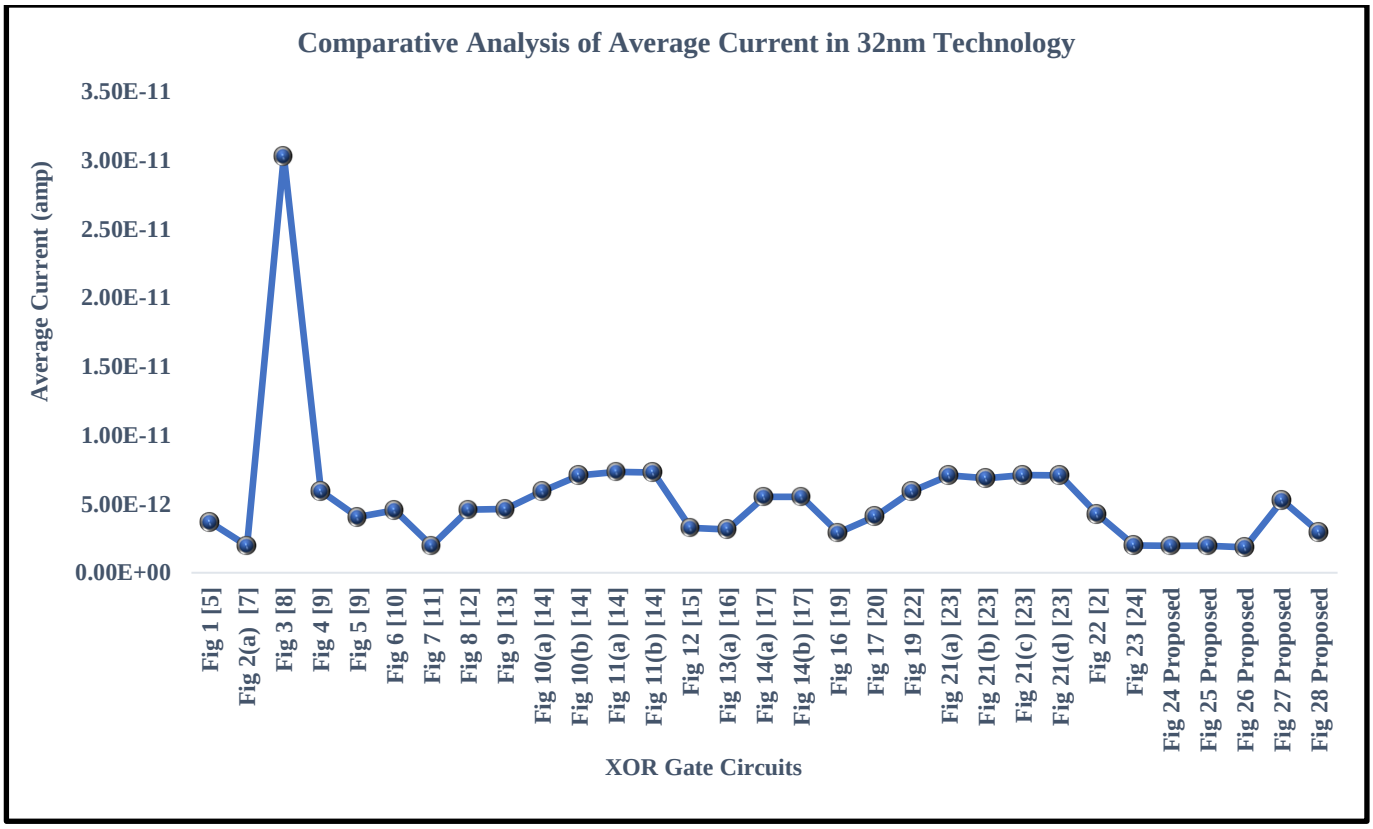

Fig. 42 Average Current Analysis of XOR Proposed design- I, II, III, IV and V with existing architectures

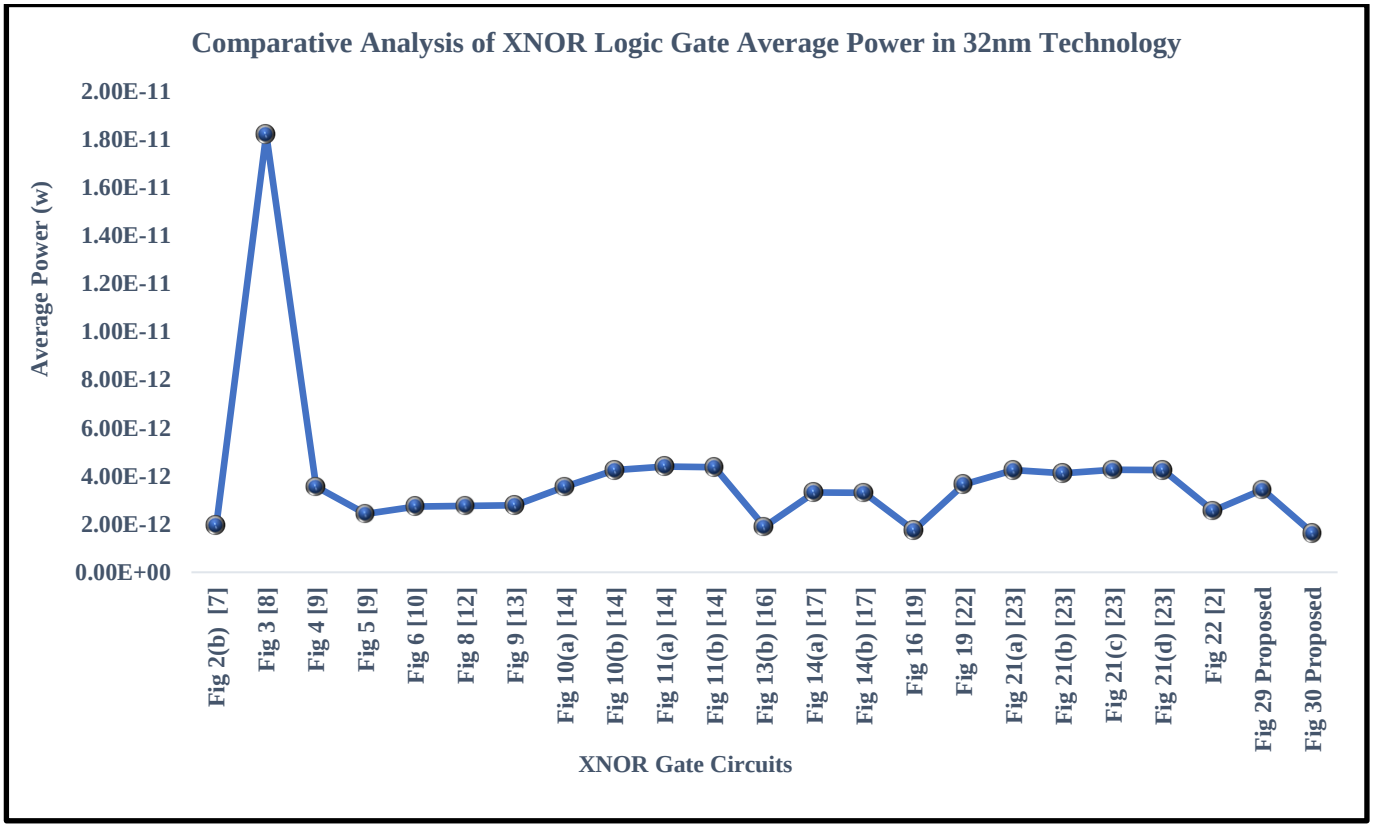

Fig. 43 Average Power Analysis of XNOR Proposed design-I and II with existing architectures

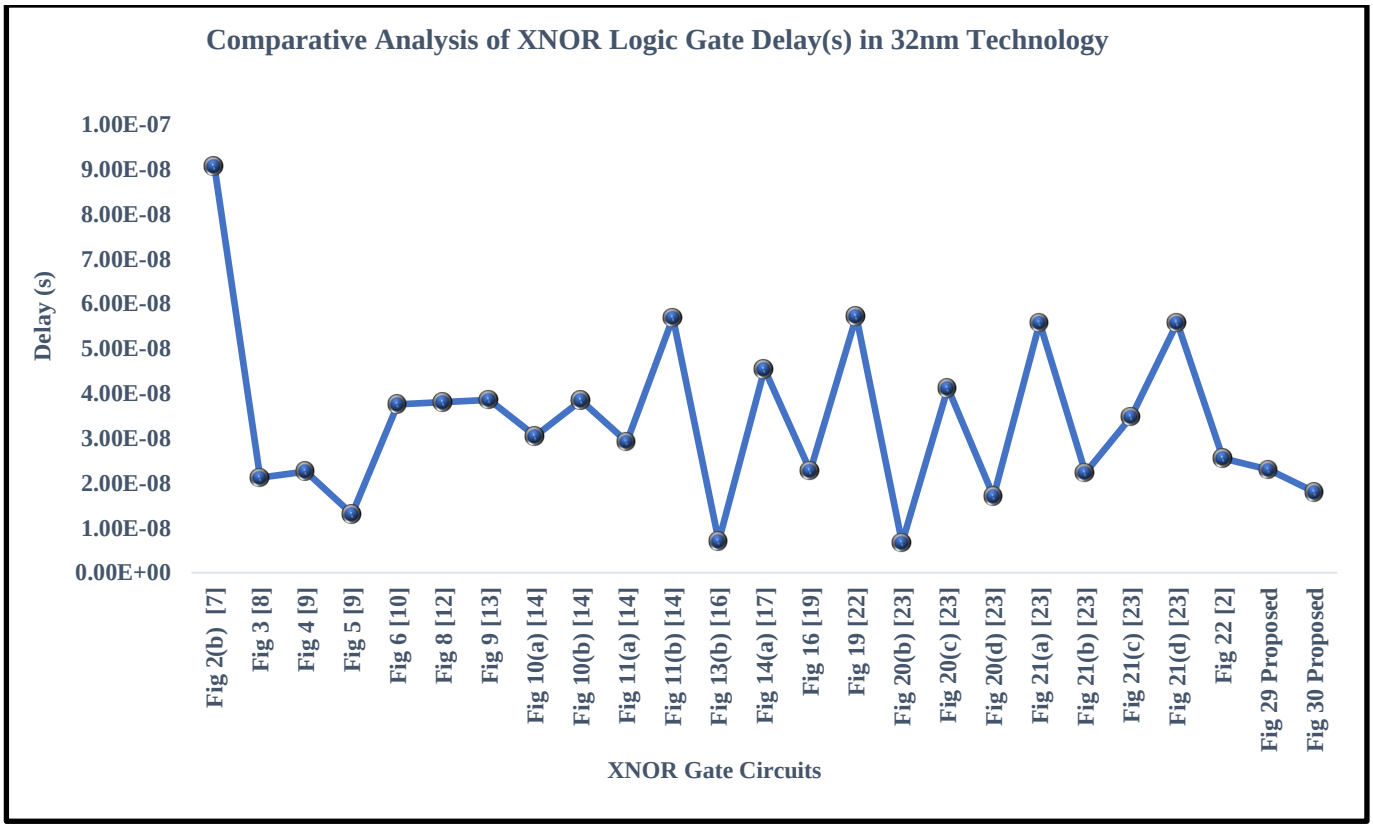

Fig. 44 Delay Analysis of XNOR Proposed design-I and II with existing architectures

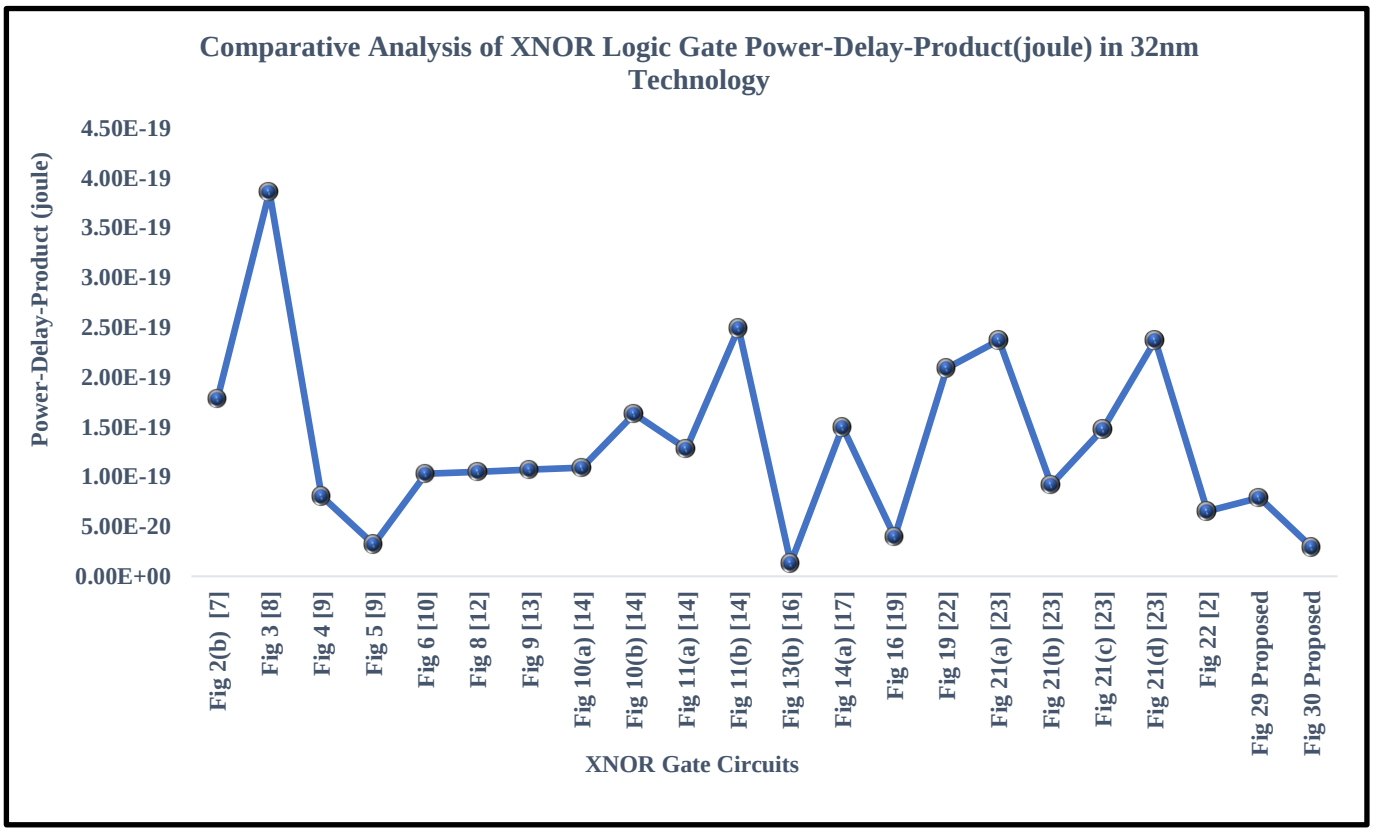

Fig. 45 Power-Delay-Product Analysis of XNOR Proposed design-I and II with existing architectures

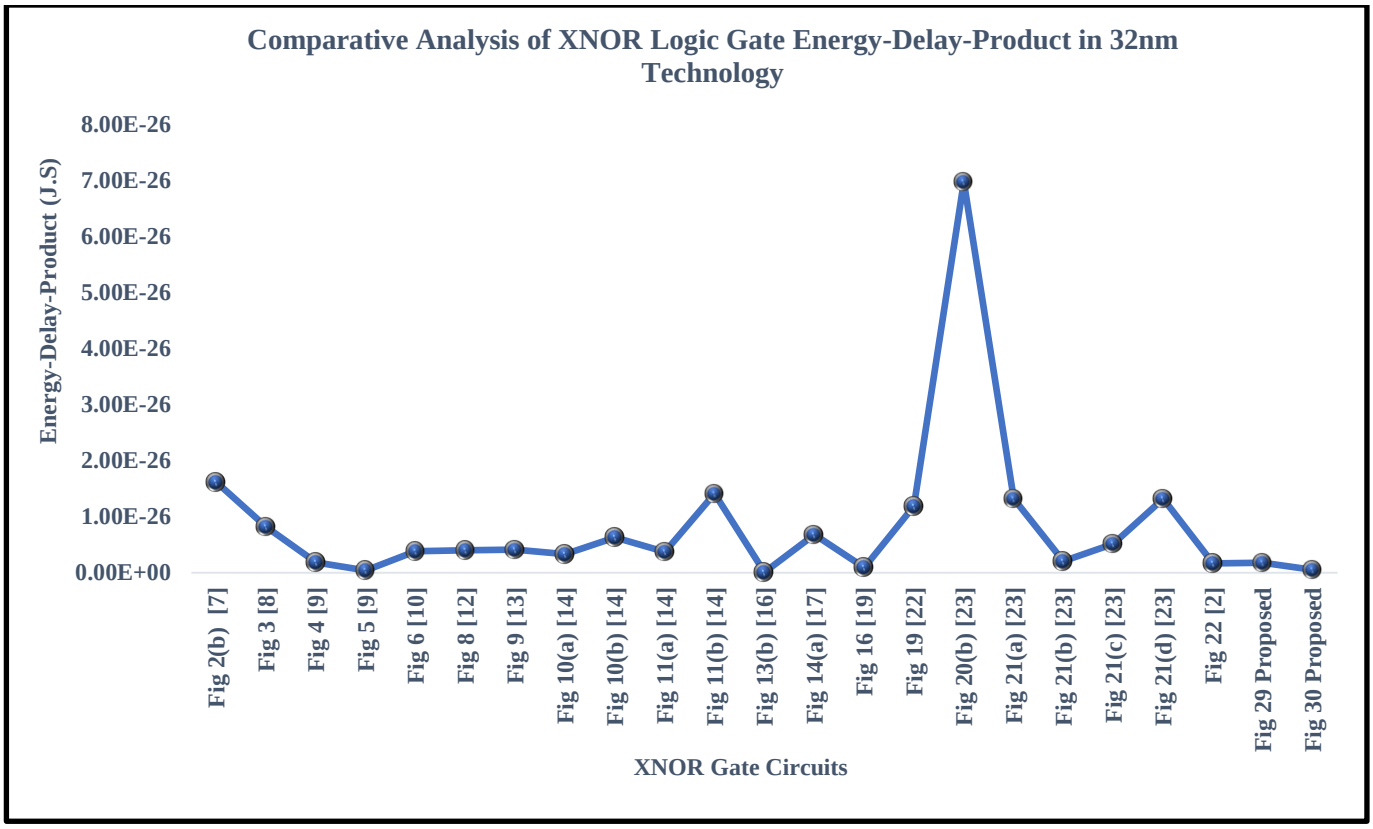

Fig. 46 Energy-Delay-Product Analysis of XNOR Proposed design-I and II with existing architectures

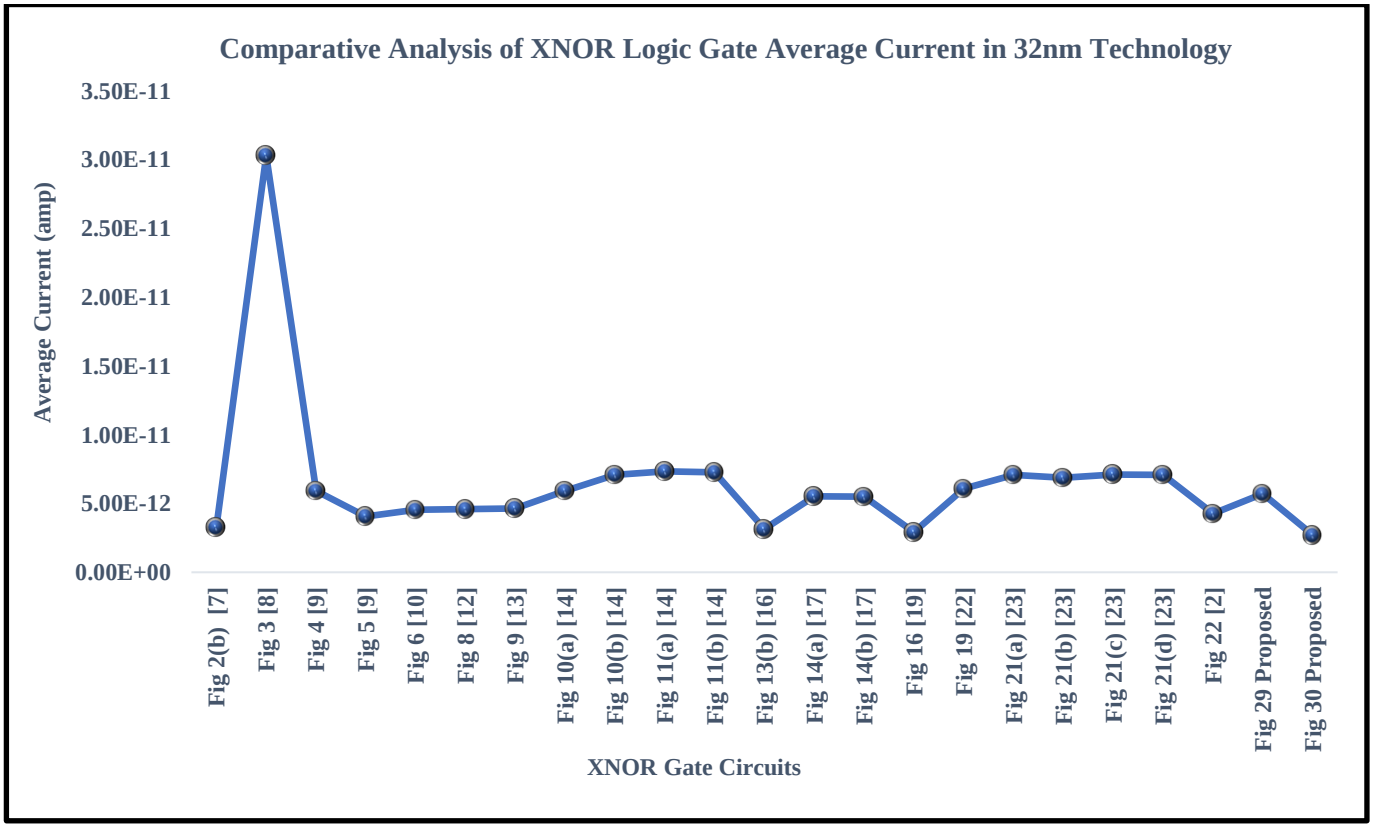

Fig. 47 Average Current Analysis of XNOR Proposed design-I and II with Existing Architectures

6. Conclusion

This research examines the many XOR and XNOR cell designs that have been reported from earlier times all the way up to the most recent ones that have been published. Following this, the paper suggests five new XOR structures and two new XNOR designs, contrasting them with existing researchers' designs on power, delay, PDP,energy-delay amalgamation, and average current. In the course of the analysis, both 32nm and 16nm technology files are employed.

The power supply is 0.6v. Earlier iterations of the XOR gate design were created using the more conventional XOR gate technology. The traditional design has a number of shortcomings, the most notable of which are an increased number of transistors, a longer latency, and a higher level of power consumption. For optimal performance, the amount of logical effort that is expended should be as low as possible. Based on the findings of the investigation, one can conclude that the XOR suggested design-III, which has only three transistors, consumes comparable low power when compared to designs that are already in use. The XOR suggested design-I, which is designed using four transistors, on the other hand, has the lowest PDP of all of the designs that have come before it.In addition, the information shown in Tables 13 and 15 allows for the drawing of the conclusion that the suggested XNOR design-II has the lowest average power and PDP compared to the other current designs. The Proposed design-II that was offered for the XNOR logic gate used four transistors. The operating capability of the suggested circuits that are shown in Figures 34 and 36 is satisfactory.

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