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Original Article

2-Bit Equality Comparator in QCA Nanotechnology Based on A New Modified Efficient EX-NOR Structures

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Abstract *- Modern integrated circuits based on CMOS gates. COMS gates have high scalability ratios according to Moore's law but with the problem of high energy consumption. One emerging solution is to use Quantum-dot Cellular Automata (QCA) nanotechnology. The data transfer and computation rely on the interaction between nearby QCA cells. Some interesting features of QCA nanotechnology, such as high speed, small size, high scalability ratios and low energy consumption, make it an alternative solution to CMOS-based logic circuits. This paper proposes a 2-bit equality comparator using two new modified QCA-based EX-NOR gates. The first proposed design structure is called the base design, while the second one is called the improved design. QCADesigner version 2.0.3 tool and QCADesigner-E tool were used to evaluate the functionality and energy consumption of the two design structures, respectively. A comparison between the two design structures shows that the improved design requires a smaller number of cells, less occupied area, less cost and less energy consumption than that for the base design, while the result shows an equal amount of delay consumed by the two designs.*

Keywords *- Energy consumption, Equality comparator, EX-NOR gate, QCADesigner, Quantum-dot Cellular Automata.*

1. Introduction

The current CMOS technology is the conventional strategy used to build and design VLSI circuits. There are three important factors that must be considered when designing VLSI circuits: the switching speed, the scaling factor and the power consumption. This technology suffers from high energy consumption due to the leakage current, which leads to low-density circuits according to the crucial factor represented by the high energy consumption of the CMOS gates, limited scalability capabilities by the oxide thickness and low switching speed technology due to diffusion barriers. Fabricating a nanoscale CMOS circuit will also increase the incompetency of designing a large-scale integrated circuit. The researchers pay attention to alternative solutions for CMOS circuit design, such as nanowire transistors, quantum material properties and quantum-dot cellular automata (QCA) [1, 2].

The new Quantum-dot Cellular Automata (QCA) nanotechnology appeared as an alternative solution to the conventional CMOS technology [3]. The QCA is a nanotechnology that provides nano-level computation circuits with low power consumption, low occupied area, high speed and high-density operations [1]. The complexity is an important factor for the validity of the computational circuits, and the QCA layouts can be optimized to decrease the circuit complexity, which depends on cell counts, occupied area and latency [3, 4]. Recently, many different digital logic circuits were implemented using QCA nanotechnology with low efficient complexity, such as the adders circuits, different types of binary comparators with different sizes, parity bit generator circuits, XOR gate implementation and many other combinational functional blocks (multiplexers, decoders, encoders) as in [5-16].

This paper proposes two new modified QCA-based EX-NOR gates to design an efficient 2-bit equality comparator, a basic building block used in arithmetic circuits as a part of CPU instructions. The proposed comparators resolve the main problems of the VLSI CMOS-based comparator circuits mentioned previously and the recent QCA-based comparator circuits. Many recent related comparator researches show different results compared to the results obtained from this research as in [6-8, 10, 16]. A comparison between the two proposed design structures and other related comparator research was achieved to demonstrate the proposed structures' validity and functionality. The comparison was made according to the number of cells, the occupied area, the cost, the circuit delay, the efficient complexity and the energy consumption.

The main contributions of this paper are twofold. First, proposing an area efficient and fast QCA-based EX-NOR gates and second, designing a 2-bit equality comparator based

on the proposed EX-NOR gate, significantly improving the performance metrics and scalability problems as explained later in the simulation results section.

The QCADesigner tool is used to design and simulate the two proposed structures and to evaluate the QCA layout parameters for each design structure [6]. The QCADesigner-E (the extended tool) is used to evaluate the total and the average amount of energy consumption for the two proposed structures [16].

The rest of the paper is organized as follows: section 2 will introduce background material, section 3 will show the proposed QCA-based Design structures for the two 2-bit equality comparators layouts, simulation results and results comparison will be shown in section 4; finally, a conclusion will be shown in section 5.

2. Background

The background material is partitioned into multiple subsections:

2.1. QCA (Quantum-Dot Cellular Automata)

Quantum-dot Cellular Automata is a lower-level abstraction that can be used to build and connect the quantum dots in several ways. The quantum dots are four dots located in the corners of a square, with two electrons enclosed in each square to represent a cell.

Due to the Coulomb interaction, the two electrons located in diagonal opposite locations, data transferring and communication are achieved via the interaction between two adjacent cells [7].

Because of the existence of two diagonals in the cell (square), they are two stable configurations of the electrons inside the cell; the configuration style is responsible for encoding the two binary logic values' 0' and '1'. Cell-to-cell interaction represents the main idea behind the data flow in QCA nanotechnology. As shown in Figure 1, there are two possible polarizations of a QCA cell [8].

As shown in Figure 1, there are two electrons in each QCA cell; the polarization (P) can be calculated as in Equation 1 [16, 17].

$$p = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4} \quad (1)$$

Where P_i represents the availability of the electron in the i'th dot. Based on the arrangements of the electrons inside the cell, the binary logic '1' can be represented as shown in Fig. 1. (a), Fig. 1. (b) shows the arrangement of the electrons inside the cell to represent binary logic '0' [9]. The following subsections introduce the basic QCA-based building blocks.

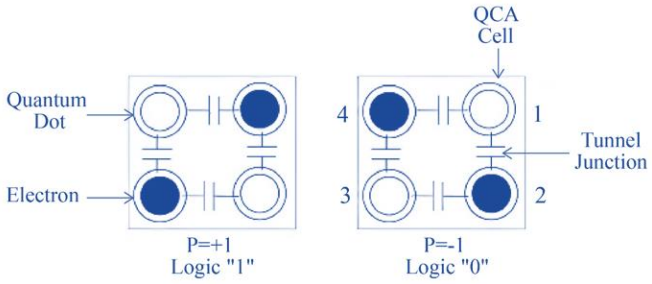

Fig. 1 QCA Cells with different polarization (a) Logic '1', (b) Logic '0'

2.1.1. QCA-based Wire

The QCA-based wire consists of multiple adjacent QCA cells arranged in a line, which transfer the binary input value to the output (last) cell [10]. The Coulomb interaction between the neighbor cells forces the cells to get the same polarization shape, which is responsible for carrying the information to the output. The QCA-based wire structure is shown in Figure 2 [1].

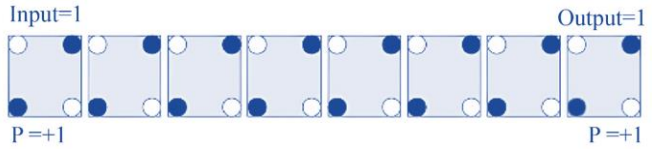

Fig. 2 QCA Wire transferring a logic '1'

Figure 2 shows 8 cells used as a QCA-based wire for transferring a logic '1' from the input of the wire to the output by using the Coulomb interaction (polarization) between the adjacent cells.

2.1.2. QCA-based Inverter

Different logic circuit diagrams can be implemented using QCA cells, and Figure 3 shows two different QCA structures of the inverter [1,8].

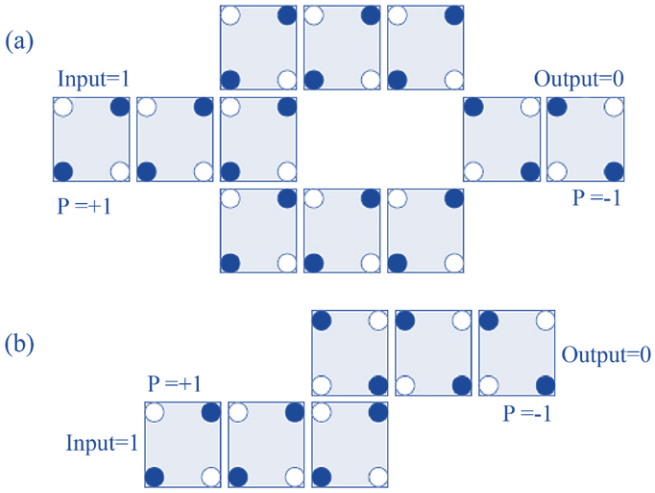

Fig. 3 Two different QCA structures for the inverter

Figure 3 shows that if the input of the inverter is equal to logic '1', the QCA cells will reverse the value of the input to logic '0' on the output [14, 15]. The structure of the inverter shown in Figure 3 (a) is more robust than that shown in Figure 3 (b).

2.1.3. QCA-Based Majority Gate

In digital logic gates, the AND gate, the OR gate and the NOT gate are the basic building gates for all logic circuit diagrams.

The QCA-based majority gate is considered the universal gate, which can be used to implement the different types of basic logic gates. Figure 4 shows the QCA cell configuration of a 3-input QCA majority gate with inputs A, B and C, and the output is F.

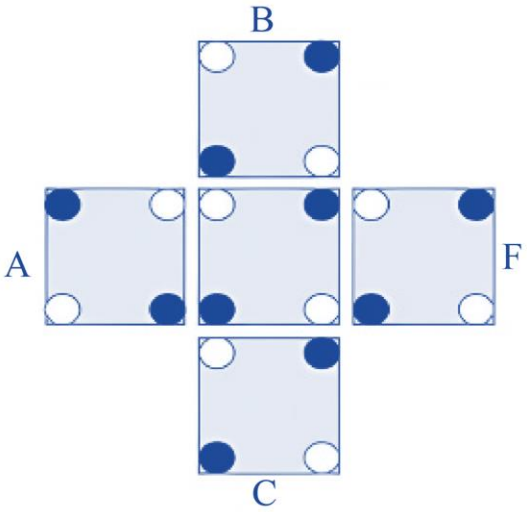

Fig. 4 Three inputs majority gate

The OR function can be implemented by applying a logic '1' value to one of the inputs, while the AND gate functionality can be implemented by applying a logic '0' to one of the inputs [16]. The general formula used for the majority gate is given by Equation 2:

$$F(A, B, C) = AB + AC + BC \quad (2)$$

Where F is the majority function for the three inputs (A, B, C).

2.1.4. QCA Clocking

In the normal case, QCA clocking is used to ensure the flow of data from the inputs of a given configuration toward the output; on the other hand, it is used to supply the needed power for the QCA cells [16, 17].

QCA introduces four clock zones, zone 0, zone 1, zone 2 and zone 3, to ensure cell switching; each zone contains four distinct clock phases: switch, hold, release and relax, as shown in Figure 5.

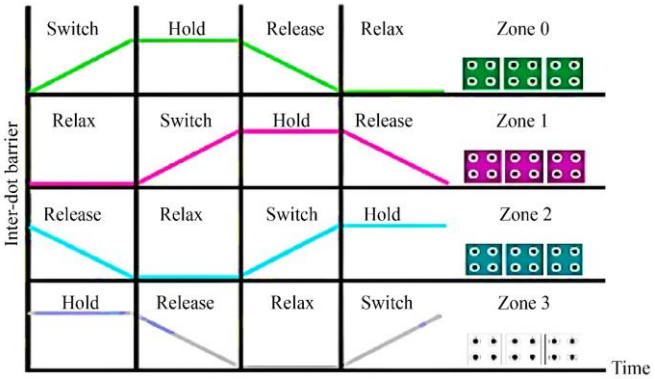

Fig. 5 QCA Clock signal with four zones

As depicted in Figure 5, each clock zone contains four phases; when clock zone 0 is in the switching phase, zone 1 will be in the relax phase, zone 2 in the release phase, and zone 3 in the hold phase. This operation and clock zone sequencing will ensure the data flow direction and switching between cells [16,18-19].

2.2. The Exclusive-NOR Gate

The XNOR gate is a logic gate that produces high output when the two inputs are equal or when the number of high inputs is even and produces low output when the two inputs are different or when the number of high inputs is odd. The XNOR gate can be called the equivalence function because the output of the gate will be high when the two inputs are equal. The Boolean equation of the XNOR gate is mentioned in Equation 3 [11-13].

$$A \text{ XNOR } B = \bar{A}.\bar{B} + A.B \quad (3)$$

Where A and B are the inputs of the XNOR gate, the truth table and the symbolic representation of the XNOR gate are shown in Table 1 and Figure 6, respectively.

Table 1. XNOR Truth table

A	B	XNOR
0	0	1
0	1	0
1	0	0
1	1	1

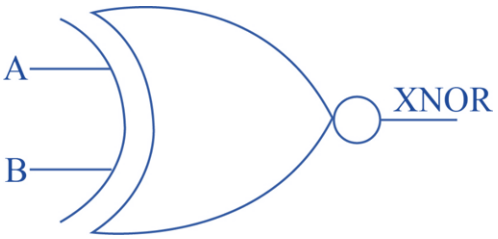

Fig. 6 XNOR Gate symbol

2.3. The 2-bit Equality Comparator

The equality comparator is a logic circuit used to check if the two inputs of a given circuit are equal or not [9]. The equality comparators used in CPUs and microcontrollers.

Some computer instructions need to decide if the contents of two registers are equal or not to take a specific action according to the result, such as the branch instructions in the MIPS assembly language instruction set. The equality comparator helps the control unit decide which instruction will be fetched next to the branch instruction.

This paper introduces a 2-bit equality comparator with two inputs, A(A_1A_0) and B(B_1B_0) and one output E. The truth table for the 2-bit equality comparator is shown in Table 2.

Table 2. 2-bit Equality comparator

A1	A0	B1	B0	E
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
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1	1	1	0	0
1	1	1	1	1

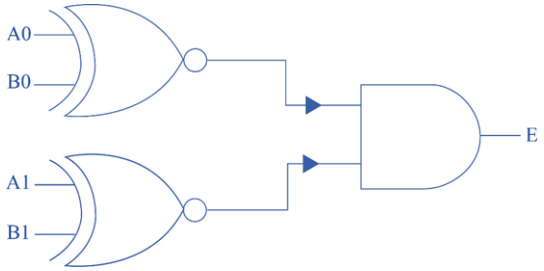

Fig. 7 The 2-bit Equality comparator logic circuit diagram

In Table 2, A_1A_0 and B_1B_0 represent the comparator inputs, while E represents the output. From Table 2., it is clear that the output E is equal to logic '1' (high) when the two inputs are equal; this case appears four times in the truth table.

The block diagram of the 2-bit equality comparator can be implemented using hierarchy to minimize the number of logic gates needed and to control the complexity of the design; as shown in Table 2, the output E must be 1 when $A_0 = B_0$ and $A_1 = B_1$, according to the equality between each corresponding bits in the input, two XNOR gates and one AND gate must be used to implement the logic circuit diagram of the 2-bit equality comparator as shown in Figure 7.

2.4. Related Works

The basic building units for all QCA-based structures are based on logic gates such as the inverter gate and the majority gate to build AND gates, OR gates and XOR gates. Recently, many researchers have been using QCA interaction to build different logic gates needed to implement their proposed design structures. The key improvement is how to find efficient individual QCA-based logic gates, such as the novel XOR gate in [4], which has a 50% speed improvement and a 35% reduction in cell count compared to the best previously reported XOR design structures. In [5], a new novel XOR gate with an optimized number of QCA cells is used to implement different multiplexers with different sizes. Different design structures for XOR and XNOR gates were mentioned in recent works to implement a variety of arithmetic functions and logical block diagrams, as in [11], which introduce novel XOR/XNOR structures used to implement a simple FPGA. Another novel XOR/XNOR structure was proposed in [14, 15]; these novel structures are used to implement different efficient circuits with significant improvement in circuit occupied area, complexity and power consumption. In [18, 19], a new XNOR structure was proposed to implement an efficient parity generator circuit.

In recent works, different comparators were introduced based on novel QCA-based XOR/XNOR structures, some of which are found in [7-10], [16]. In [20], a novel XOR design structure was proposed to implement a 1-bit comparator circuit, 1-bit full adder, binary to gray and gray to binary converters. In this paper, two new design structures of XNOR gates are proposed to implement a 2-bit equality comparator; the two XNOR-based equality comparators will be compared and verified using QCADesigner and QCADesigner-E tools.

3. The Proposed Structures and Design

This paper proposes two different 2-bit equality comparators based on two different QCA-based XNOR gate structures.

3.1. XNOR Structures

This paper introduces two different structures for the XNOR gate function. The first structure is called the base structure, and the second is called the improved structure.

3.1.1. The base XNOR Structure

This structure is based on the XOR structure proposed in [5] with some modifications to perform the XNOR functionality needed as shown in Figure 8, where a0 and b0 are the inputs of the XNOR gate, while output is the output of the XNOR gate.

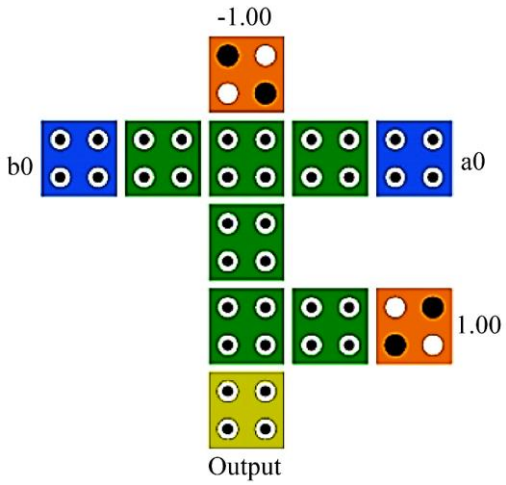

Fig. 8 The proposed QCA-based XNOR structure (base design)

3.1.2. The improved XNOR Structure

The proposed structure of the improved XNOR gate is based on the design structure in [4], with some modifications achieved to perform the logical function of the XNOR gate. Figure 9 shows the QCA-based structure of the improved XNOR structure.

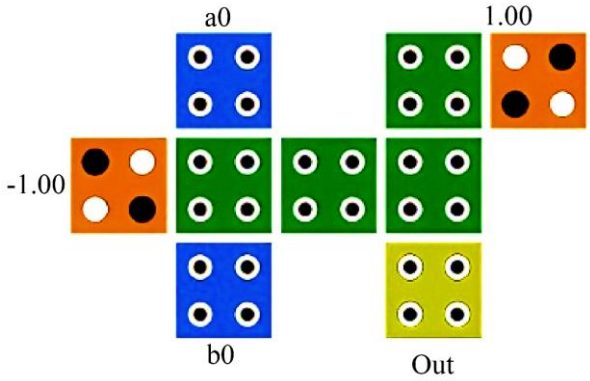

Fig. 9 The proposed QCA-based XNOR structure (improved design)

Where a0 and b0 are the inputs of the XNOR, while the out is the output of the proposed improved XNOR gate structure.

3.2. The Proposed 2-bit Equality Comparator Design

The 2-bit equality comparators introduced in this paper are organized into two subsections: the first design structure is called the base 2-bit equality comparator design structure, and the second design is named the improved 2-bit equality comparator design structure.

3.2.1. The base 2-Bit Equality Comparator Design Structure

The proposed QCA-based base design of the 2-bit equality comparator is shown in Figure 10.

The structure shown in Fig.10 has four input variables named: a0, b0, and a1 and b1and one output signal named out.

The output of the structure shown in Figure 10 will be high if the two inputs (a1 a0) and (b1 b0) are equal; the output of the comparator will be low. The structure in Figure 10 is assembled from two base XNOR structures shown in Fig. 8 and from one AND gate implemented using the QCA-based 3-input majority gate connecting the two XNOR outputs based on the design shown in Figure 7. The proposed structure in Figure 10 is implemented using 29 QCA cells with two clock zones (clock zone 0 and clock zone 1) to achieve the required output.

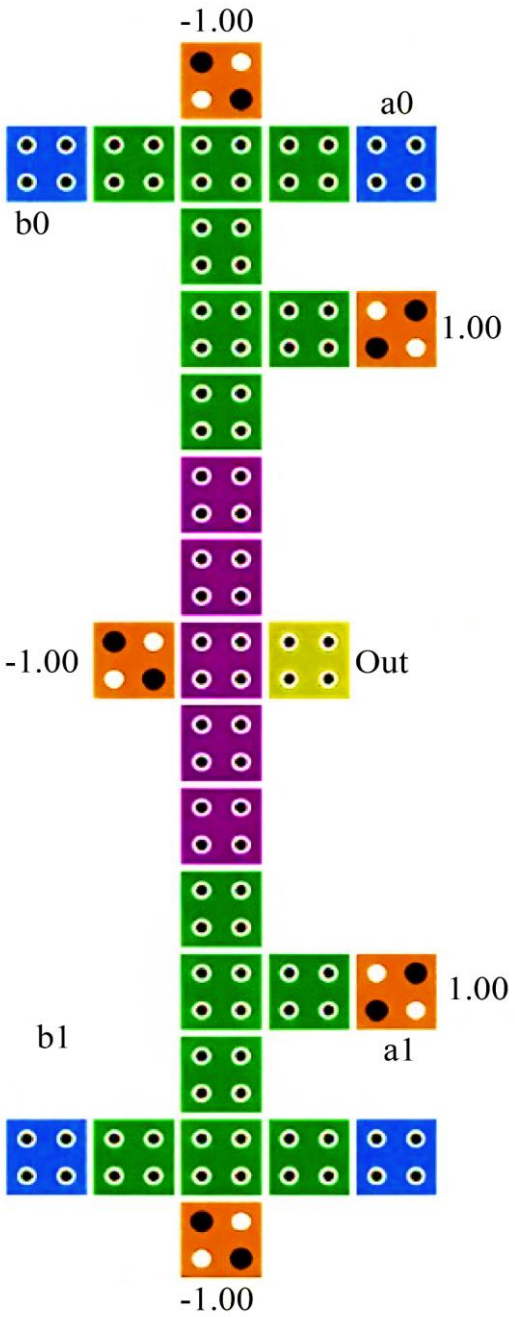

Fig. 10 The base 2-bit equality comparator structure

3.2.2. The improved 2-bit Equality Comparator Design Structure

The proposed improved QCA-based design structure of the 2-bit equality comparator is shown in Figure 11.

Figure 11 consists of two XNOR gates and one AND gate connected based on the circuit diagram shown in Figure 7; the XNOR design structure in Figure 9 is used to implement the comparator. The 3- input majority gate shown in Figure 4 is used to implement the AND gate to achieve the required functionality of the comparator.

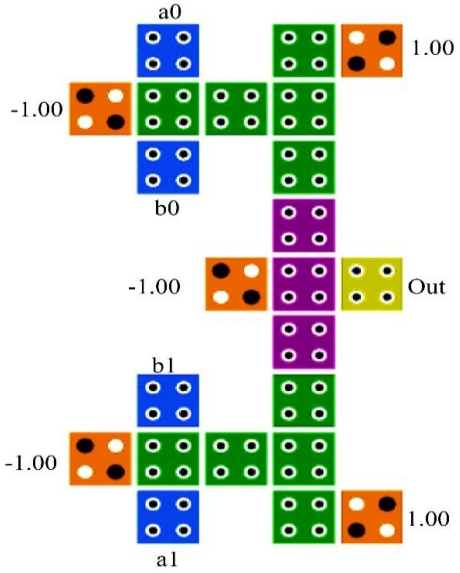

Fig. 11 The improved 2-bit equality comparator structure

The QCA-based structure of the comparator shown in Figure 11 has four inputs, (a1 a0) and (b1 b0) and an output line named (out). The output of the comparator will be high when the two inputs are equal, while the output will be low when they are different. The comparator structure shown in Figure 11 has 23 QCA cells using two clock zones (clock zone 0 and clock zone 1) to achieve the required output.

As shown in Figure 10 and Figure 11, both design structures were implemented using two XNOR gates and one AND gate, but the main difference between them is in the QCA-based structure of the XNOR gate used in each case.

4. Simulation Results and Comparison

The QCADesigner tool version 2.0.3 is a well-known simulation tool for creating and implementing logical circuit diagrams using QCA cells. This simulation tool implements the two design structures proposed in this paper. The QCADesigner has the capability to evaluate the validity and functionality of the logic circuit diagram, such as the 2-bit equality comparator proposed in this paper [23]. The two proposed designs achieved under simulation parameters are shown in Table 3.

The QCADesigner-E tool is an extension of the QCADesigner 2.0.3. It implements QCA-based logic circuits and assists their total energy consumption and the average energy consumption by a given logic circuit design [24]. The standard parameters of the tool were used to evaluate the total and the average amount of energy consumption by the 2-bit equality comparator for the two design structures.

Table 3. Simulation parameters

Parameter	Value
Cell width	18 nm
Cell height	18 nm
Relative permittivity	12.9
Dot diameter	5 nm
Number of samples	12,800
Convergence tolerance	0.001
Clock high	9.8X 10-22 J
Clock low	3.2 X 10-23 J
Clock amplitude factor	2
Radius of effect	56 nm
Layer separation	11.5 nm
Maximum iteration per sample	100

4.1. Simulation Results of the Base Structure

The simulation results of the base design structure are shown in Figure 12.

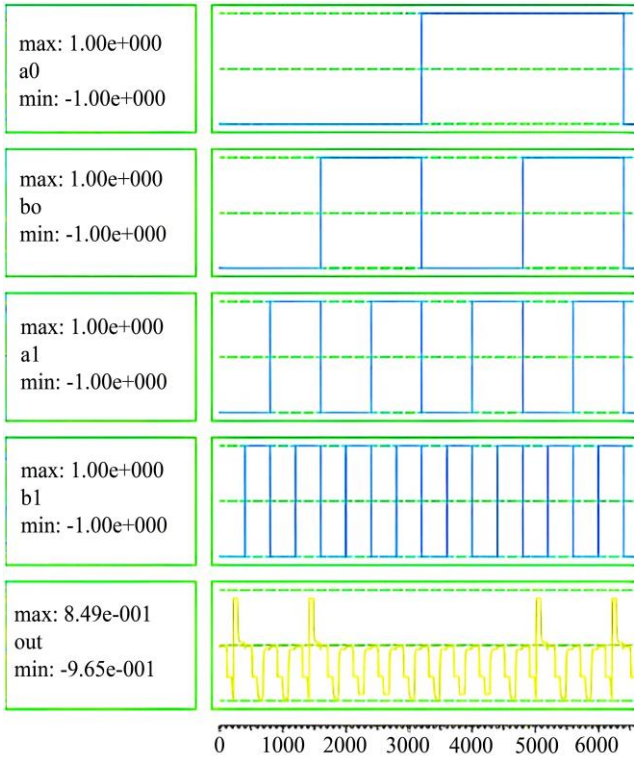

Fig. 12 Simulation results for the base design 2-bit equality comparator

As shown in Figure 12, the 2-bit equality comparator has two inputs, A and B; each input consists of two bits (a0 a1) and (b0 b1); the output is named out. From the simulation results shown in Figure 12, it can be seen that the output (out) is high when the inputs are equal, which occurs four times during each cycle when the inputs are equal to (a1a0 = b1b0 = 00, 01, 10 and 11). The results taken from the simulation output prove the functionality of the 2-bit equality comparator compared to the data shown previously in Table 2. In addition, the simulation result shows that the output is correctly obtained after a 0.5 clock cycle delay from the current inputs.

4.2. Simulation Results of the Improved Structure

The simulation results of the improved design structure of the 2-bit equality comparator are shown in Figure 13, which shows that the proposed 2-bit equality comparator has two inputs, A and B, with two bits for each (a0 a1) and (b0 b1), and one output named (out). The simulation result shown in Figure 13 shows that the output is equal to high when the two inputs are equal, which occurs at four input combinations at a1a0 = b1b0 = 00, 01, 10 and 11, while the output is low when the two inputs are different. These results achieve the logical functionality of the equality comparator mentioned in Table 2.

From Figure 13, the simulation result shows that the output is achieved after a delay of 0.5 clock cycles from the inputs, which is the same amount of delay achieved by the base design structure of the 2-bit equality comparator mentioned in the previous section.

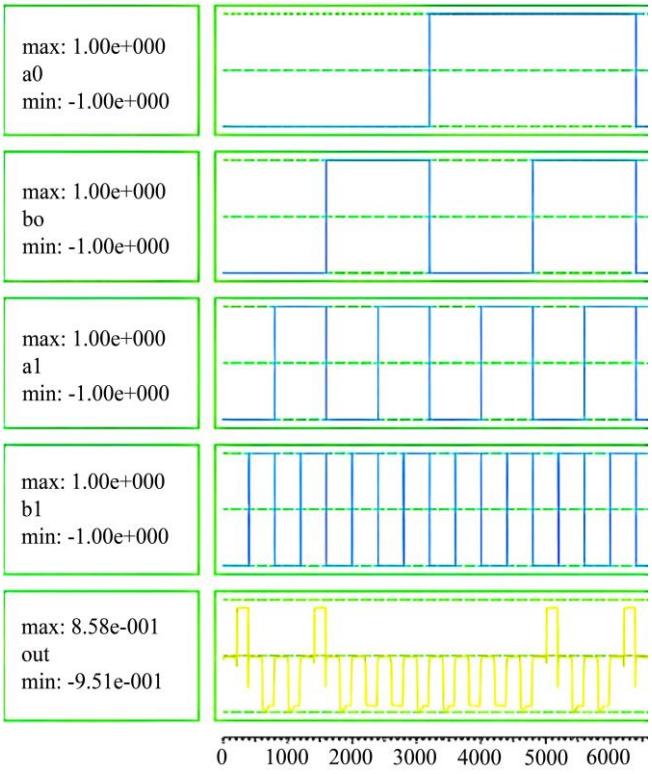

Fig. 13 Simulation results for the improved 2-bit equality comparator

A complete comparison between the two design structures of the 2-bit equality comparator is introduced in detail in the next section.

4.3. Comparison Between the Two Design Structures

Both design structures were implemented using the QCADesigner tool and the QCADesigner-E tool with valid functionality, as the simulation results show in Fig. 12 and Figure 13. According to these results, the base design was implemented using 29 QCA cells with 0.055 μm^2 occupied area, and the output was taken after a delay of 0.5 clock cycles from the inputs.

In order to compare the two design structures with respect to their energy dissipation, the QCADesigner-E tool is used; the base design of the 2-bit equality comparator dissipates a total amount of energy of about 0.0212 (eV) and an average energy dissipation of about 0.00193 (eV) which is considered as low average energy dissipation level.

The improved design structure of the 2-bit equality comparator achieves better results compared to the base design structure with 23 QCA cells used to perform the logical functionality of the comparator. It occupies 0.046 μm^2 area with output delayed by 0.5 clock cycles from the inputs. The proposed improved design structure dissipates a total energy of 0.011 (eV), while the average amount of energy dissipation is about 0.001 (eV). A clear, complete comparison between the two design structures according to different circuit parameters is shown in Figure 14, Figure 15 and Figure 16.

Figure 14 compares the two structures based on their number of cells and their occupied area; as shown in Figure 14, the improved design structure achieves a reduction in the number of QCA cells used to implement the design and a reduction in the area occupied by the design structure.

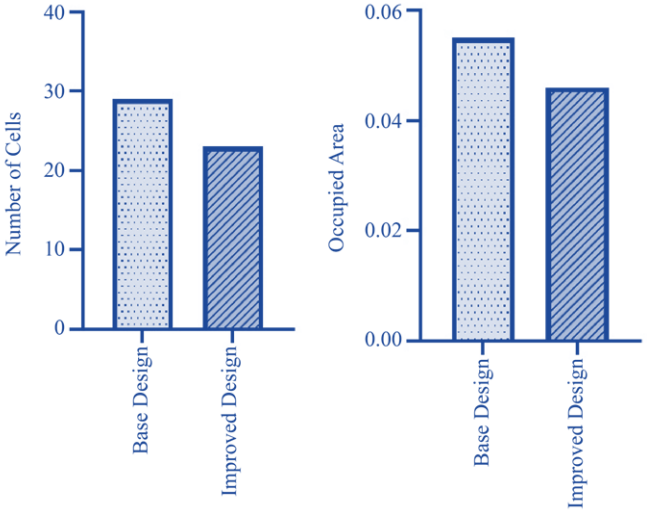

Fig. 14 Comparison of (a) Number of cells, (b) Occupied area of the two proposed structures

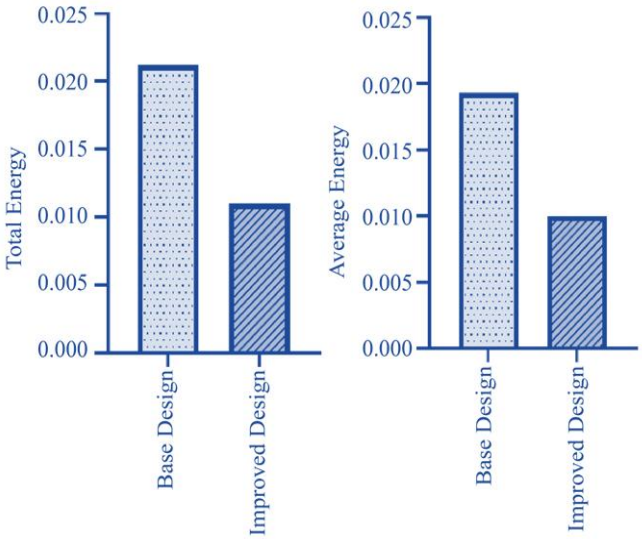

Fig. 15 Energy comparison for the two structures (a) Total energy (b) Average energy

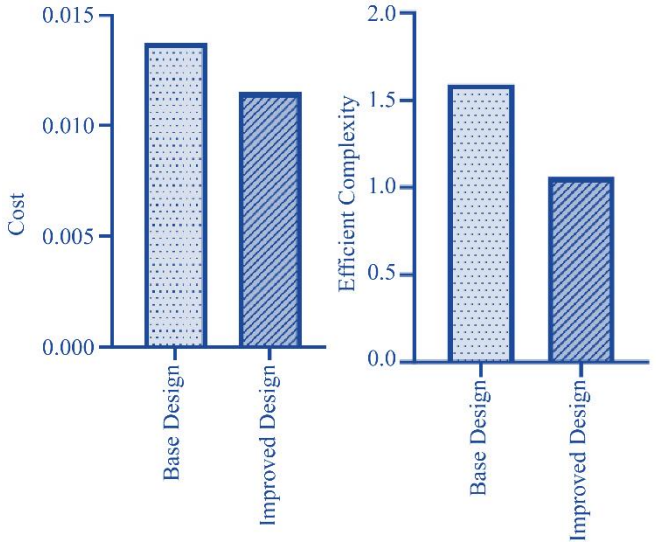

Fig. 16 Comparison according to (a) Cost (b) Efficient complexity

The percentage improvement for the improved design according to the number of QCA cells used is 21% over the number of QCA cells used to implement the base design structure, while the percentage improvement according to the occupied area is 16.3%.

Figure 15 compares the two design structures based on the total amount of energy consumption and the average amount of energy consumption by the two design structures.

As seen from Figure 15 (a), the improved design structure has lower total energy than the base design structure, with a 48.1% percentage reduction improvement according to a low number of QCA cells used during the implementation. The average amount of energy dissipation values shown in Figure 15 (b) shows significant reduction improvement reaches 48.3%.

The cost and the efficient complexity of the QCA-based logic circuit diagrams can be used to evaluate the results taken from a given design structure. The cost of a given QCA-based circuits can be simply calculated by multiplying the occupied area of the circuit by the square of its latency (delay), as shown in Equation 4 [6].

$$Cost = Area \times latency^2 \quad (4)$$

The efficient complexity for a given QCA-based circuit is calculated by multiplying the number of QCA cells by the occupied area of the circuit by the power of the reciprocal of the number of QCA layers used as given in Equation 5 [6].

$$Efficient\ Complexity = Number\ of\ Cells \times Area^{1/n} \quad (5)$$

Where n is the number of QCA layers used. For comparison purposes, the cost and the efficient complexity of the two design structures are shown in Figure 16.

Figure 16 (a) shows that the improved design structure has less cost than the base design structure, which achieves a reduction improvement in cost of 16.3% compared to the cost of the base design structure. From Figure 16 (b), it is clear that the improved design structure has less efficient complexity compared to the efficient complexity for the base design structure; the efficient complexity reduction improvement percentage reaches 33.4% compared to the based design structure.

Table 4 summarises the performance metrics of the proposed comparator designs.

Table 4. Proposed structures comparison summary

Design	Base Design	Improved Design
Cell Counts	29	23
Area (μm^2)	0.055	0.046
Delay (clock cycles)	0.5	0.5
Total energy (eV)	0.0212	0.011
Average energy (eV)	0.00193	0.001
Cost	0.01375	0.0115
Efficient Complexity	1.595	1.058

It is worth noting that although several research efforts have tackled the design of QCA-based comparators [6-8, 10, 16], this work is among the first efforts to propose a 2-bit QCA-based equality comparator, to the best of the author's knowledge.

5. Conclusion

This paper proposes two new efficient XNOR gate design structures with an optimized number of QCA cells to implement the design of a 2-bit equality comparator. The first design structure is called the base design, and the second one is called the improved design. A comparison between the two structures was made to verify and evaluate the functionality and the validity of the two structures by using the

QCADesigner tool. In order to evaluate the total amount and the average amount of energy dissipated by the two structures, the extension version QCADesigner-E tool is used for this purpose.

As cleared in simulation results, the improved design structure achieves better results compared to the base design structure based on some evaluation factors like cell count, occupied area, circuit delay, cost and efficient complexity. The proposed improved design structure introduces a 21% percentage improvement in QCA cell count compared to the base design, while the percentage improvement was 16.3% for both designs with respect to occupied area and cost. On the other hand, the proposed improved design achieves 48.1% and 48.3% percentage improvements in total and average energy dissipation compared to the base design structure, respectively. In addition, the improved design has a 33.4% improvement in terms of efficient complexity. These results provide a good chance to improve a complete n-bit comparator.

References

[1] Trailokya Nath Sasamal, Ashutosh Kumar Singh, and Anand Mohan, *Quantum-dot Cellular Automata Based Digital Logic Circuits: A Design Perspective*, Springer Nature, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[2] Sadat Riyaz, and Vijay Kumar Sharma, "Design of Reversible Feynman and Double Feynman Gates in Quantum-dot Cellular Automata Nanotechnology," *Circuit World*, vol. 49, no. 1, pp. 28-37, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[3] C.S. Lent et al., "Quantum Cellular Automata," *Nanotechnology*, vol. 4, no. 1, 1993. [CrossRef] [Google Scholar] [Publisher Link]

[4] Ali H. Majeed et al., "Full Adder Circuit Design with Novel Lower Complexity XOR Gate in QCA Technology," *Transactions on Electrical and Electronic Materials*, vol. 21, pp. 198-207, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[5] Li Xingjun et al., "A New Design of QCA-based Nanoscale Multiplexer and Its Usage in Communications," *International Journal of Communication Systems*, vol. 33, no. 4, p. e4254, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[6] Ziyad A. Altarawneh, and Mutaz A.B. Al-tarawneh, "Design and Analysis of Single Layer Quantum Dot-cellular Automata based 1-bit Comparators," *Telkomnika*, vol. 20, no. 1, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[7] Mohsen Vahabi et al., "Novel Reversible Comparator Design in Quantum-dot Cellular Automata with Power Dissipation Analysis," *Applied Sciences*, vol. 12, no. 15, p. 7846, 2022. [CrossRef] [Google Scholar] [Publisher Link]

[8] Ahmadreza Shiri, Abdalhossein Rezai, and Hamid Mahmoodian, “Design of Efficient Coplanar 1-bit Comparator Circuit in QCA Technology,” *FACTA Universitatis-Series: Electronics and Energetics*, vol. 32, no. 1, pp. 119-128, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[9] Vijay Kumar Sharma, "Optimal Design for Digital Comparator using QCA Nanotechnology with Energy Estimation," *International Journal of Numerical Modeling*, vol. 34, no. 2, p. e2822, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[10] A. Mallaiah, G.N. Swamy, and K. Padmapriya, "1-bit and 2-bit Comparator Designs and Analysis for Quantum-dot Cellular Automata," *Nanojournal: Russia*, vol. 8, no. 6, pp. 706-716, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[11] A. Kartheeswari et al., "A Novel Coplanar-based XOR/XNOR Structure for Designing QCA Circuits," *International Journal of VLSI and Signal Processing*, vol. 8, no. 1, pp. 21-23, 2021. [CrossRef] [Publisher Link]

[12] Deng Fengbin et al., "A Novel Design and Analysis of Comparator with XNOR gate for QCA," *Microprocessors and Microsystems*, vol. 55, pp. 131-135, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[13] K. Bharathi, and S. Vijayakumar, "QCA Design of Encoder for Low Power Memory Applications," *SSRG International Journal of Electronics and Communication Engineering*, vol. 3, no. 11, pp. 13-15, 2016. [CrossRef] [Publisher Link]

[14] Lei Wang, and Guangjun Xie, "A Novel XOR/XNOR Structure for Modular Design of QCA Circuits," *IEEE Transaction on Circuits and Systems II: Express Briefs*, vol. 76, no. 12, pp. 3327-3331, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[15] Rashmi Chawla et al., "A5/1 Algorithm Based On Quantum-Dot Cellular Automata (QCA) Technology," *International Journal of P2P Network Trends and Technology*, vol. 5, no. 1, 2015. [CrossRef] [Publisher Link]

[16] Ali Hussien Majeed et al., "Single-bit Comparator in Quantum-dot Cellular Automata (QCA) Technology using Novel QCA -XNOR Gates," *Journal of Electronic Science and Technology*, vol. 19, no. 3, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[17] Yash Bishnoi et al., "Review Shop Store Quantum-Dot Cellular Automata," *SSRG International Journal of VLSI & Signal Processing*, vol. 8, no. 1, pp. 1-4, 2021. [CrossRef] [Publisher Link]

[18] Vijay Kumar Sharma, "Parity Generators for Nano Communication Systems using QCA Nanotechnology," *Periodica Polytechnica Electrical Engineering and Computer Science*, vol. 67, no. 2, pp. 229–237, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[19] Ratna Chakrabarty, Anisha Paul, and Ankita Majumder, "Design of an Alphanumeric Symbol Encoder Circuit using Quantum Dot Cellular Automata," *SSRG International Journal of Electrical and Electronics Engineering*, vol. 3, no. 11, pp. 1-7, 2016. [CrossRef] [Publisher Link]

[20] Behrouz Safaiezadeh et al., "Design and Simulation of Efficient Combinational Circuits based on a New XOR Structure in QCA Technology," *Optical and Quantum Electronics*, vol. 53, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[21] Ziyad Altarawneh, and Mutaz Al-tarawneh, "Improved QCA-based Full Adder/Subtractor Structures," *International Review of Electrical Engineering*, vol. 16, no. 4, pp. 391-400, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[22] Mutaz Al-tarawneh, and Ziyad Altarawneh, "C-element Design in Quantum Dot Cellular Automata," *Jordanian Journal of Computers and Information Technology*, vol. 7, no. 1, pp. 52-64, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[23] K. Walus et al., "QCA Designer: A Rapid Design and Simulation Tool for Quantum-dot Cellular Automata," *IEEE Transactions on Nanotechnology*, vol. 3, no. 1, pp. 26-31, 2004. [CrossRef] [Google Scholar] [Publisher Link]

[24] Frank Sill Torres et al., "An Energy-aware Model for the Logic Synthesis of Quantum-dot cellular Automata," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 12, pp. 3031-3041, 2018. [CrossRef] [Google Scholar] [Publisher Link]