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Original Article

Parametric Analysis of Prototyped Differential Amplifier using Double-Gate MOSFET

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Abstract *- A differential amplifier using Double-Gate (DG) MOSFET has been designed in this research work. The designed MOSFET-based differential amplifier uses BF998 MOSFET because of its capacity to reduce Short-Channel Effects (SCE) and gate current leakage. The basic information and operation of DG MOSFET and differential amplifier have been discussed. Mathematical modeling has been performed to analyze the designed differential amplifier to evaluate its performance parameters such as (i) single input – single out the gain, (ii) single input differential output voltage gain, (iii) common-mode input gain, (iv) common mode rejection ratio (CMRR),(v) frequency response, and (vi) comparative analysis. The single input – single output voltage gain, single input – differential output voltage gain, common-mode gain (differential output), common mode rejection ratio, and frequency response simulation results were obtained as -6.8 V/V, -13.1 V/V, 39 µV/V, 67.18 kV/V, and 60 MHz, respectively. This model is suitable for low-power / energy devices.*

Keywords *- Prototype design, Double-gate MOSFET, Differential amplifier, Low-power /Energy device, Microelectronics, Nanotechnology, VLSI.*

1. Introduction

The MOSFET is the most common basic cell in both digital and analog circuits. The development of differential amplifiers is among the most common applications of MOSFETs in analog circuits. These are used as input stages in operational amplifiers, video amplifiers, high-speed comparators, and various other analog-based circuits [1-3]. MOSFET differential amplifiers, such as operational amplifiers, are used in integrated circuits because they have a high input impedance [4]. Furthermore, they generate a linearly amplified output signal while rejecting the common component of the two input signals [4, 5]. Hashem [6] has designed and analyzed a differential amplifier using NMOS transistor differential amplifier circuit with a passive load that uses a modified Wilson current mirror as a biasing circuit. The output resistance of the current mirror was 2.297 MΩ. The differential amplifier's CMRR, output resistance, and power dissipation were 33.351 dB, 61,274 kΩ, and 6.66 mW, respectively. Ruj and Singh [7] have designed and analyzed a MOSFET differential amplifier using the NG Spice tool. The improved differential gain of 5 dB was achieved. Aderao and Sushmakejgir [8] have designed a CMOS multi-staged high-gain differential amplifier. In that work, a second stage was used because the amplified signal did not meet op-amp requirements, which improved the amplifier's gain. Almusallam and Ashkanani [9] have discussed the design of differential amplifiers using CMOS technology. The design presented its optimized architecture using 0.18-µm technology and a supply voltage of 1.8 V.

Shilpa and Srilatha [10] have designed and analyzed a high-gain differential amplifier using various topologies. The gain, CMRR, and gain bandwidth products were analyzed. The designs were operated at 1.8 V using 0.18-µm technology. Prasath and Aruna [11] have designed different low-noise amplifiers with lumped, distributed, and RF chokes to achieve better noise immunity and gain. The achieved gain and noise figures were 3.2 dB and 1.468 dB, respectively. Kakarla and Alagirisamy [12] have designed a low-power operational amplifier using 18-nm technology for biomedical applications. Power and timing analysis was done in that work, and the results showed a significant improvement compared to other traditional amplifiers. Sudharshan and Divakar [13] designed and simulated an error amplifier using power management chips. In that work, the simulated amplifier used a high gain of 60 dB, UGB of 75 MHz, PSRR of -83 dB, and slew rate of 54 V/µs which was able to make errors low.

An et al. [14] have designed a capacitors DRAM based on a Polycrystalline-Silicon dual-gate MOSFET with a fin-shaped structure. The proposed 1T-DRAM cell exhibited a sensing margin of 2.51 µA/µm and retention time of 598 ms at T = 358 K. Gelao et al. [15] have analyzed the limits of CNTFET devices with the behavior of a differential amplifier based on CNTFET for application between 50 GHz and 500 GHz, determining the highest gain achievable with the low noise level.

Sahani et al. [16] have designed an operational transconductance amplifier using Double-Gate (DG) MOSFET. This double gate-based circuit provided an additional gain in power and speed and achieved a gain and bandwidth of 9.32 dB and 7 GHz, respectively. Kadam and Kulkarni [17] have designed and analyzed a DG MOSFET operational amplifier in 45-nm technology. This design analyzed the active and passive load for gain and power dissipation. The symmetrically driven double-gate and independently driven double-gate MOSFET were designed and realized to find the best topology. It was found that an Independently Driven Double-Gate (ID DG) based operational amplifier was better than a Symmetrical Driven Double-Gate (SD DG) based. A gain of 27 dB and power dissipation of 157.8 μW was achieved. Roy et al. [18] have performed a circuit performance analysis of the DG MOSFET's graded doping with a high-k gate stack for analog and digital applications. The DG MOSFET's source and drain were doped in different concentrations. The digital and analog performance of the device was realized by implementing 6T SRAM and a differential amplifier. Maqsood and Rao [19] have realized an analog circuit using DG MOSFET at 32-nm technology. An analog circuit, such as a CMOS amplifier, was analyzed. Tai et al. [20] have designed a differential amplifier with the top gate as an input to boost the gain. It was obtained that the gain increased 3.5 times compared to other conventional single-gate IGZO TFTs. Pillay and Srivastava [21] designed a DG MOSFET-based class-AB amplifier. It concluded that DG MOSFET is superior in power applications because it produces noticeable output power. Pillay and Srivastava [22] designed an active-loaded differential amplifier using DG MOSFET.

To extend the work on the differential amplifier design, this present research aims to design and analyze a DG MOSFET-based differential amplifier. It has the ability to reject common signals and amplify the difference between the two input signals. The main focus is low-power applications with common parameters, i.e., differential gain, common mode gain, bandwidth, and CMRR. This research paper has been organized as follows. Section 2 discusses the basic theories of the DG MOSFETs and the differential amplifier. Section 3 represents the modeling of the system, which is applied to the design. Section 4 has the designed circuit of the DG MOSFET-based differential amplifier. Section 5 details the parametric and simulated results analysis. Finally, Section 6 concludes the work and recommends future aspects.

2. Design Methodology and Materials

2.1. Double-Gate (DG) MOSFET and Its Operation

The DG MOSFET is a distinctive modification of the standard MOSFET design that employs two gates to control the channel rather than the usual single gate. It has much potential for nanometer-scale transistors in extremely congested IC designs. The DG MOSFET's essence consists of putting two gate terminals at the top and bottom of the channel in an extremely thin SOI body, enabling effective gate control over the channel on both gates [22-24]. Both gates in a double gate device are paired to each other, which reduces the short channel effect and leakage. Compared to the planer CMOS circuit, the two gates circuit with a double-gate transistor can be operated with a lower input voltage, resulting in lower power consumption [22].

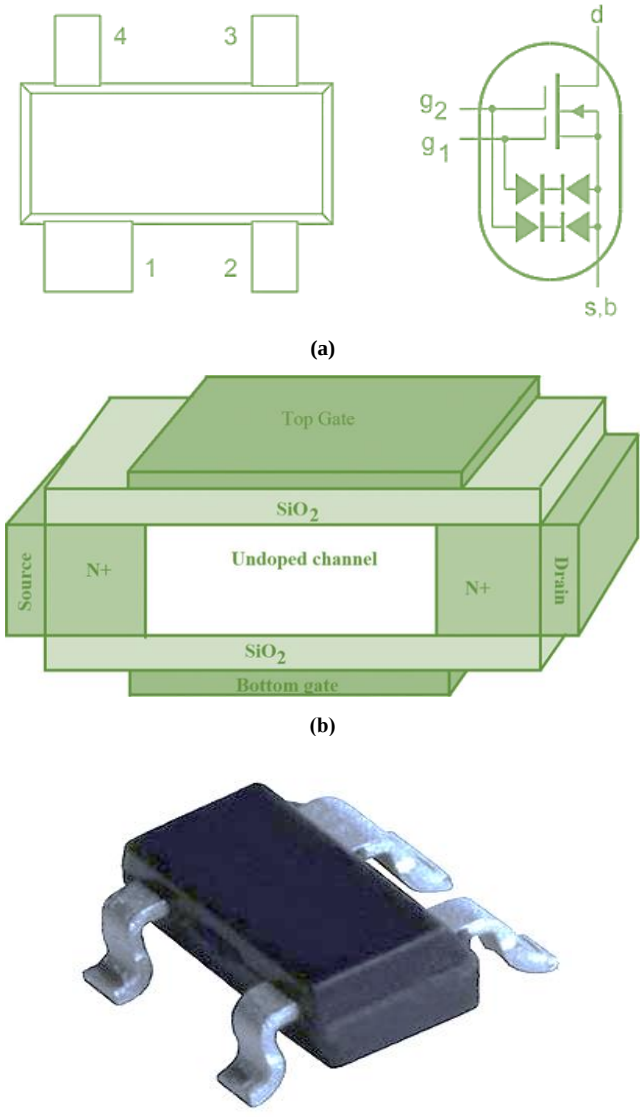


Fig. 1 (a) Double-gate MOSFET Structure, (b) BF998 double-gate MOSFET pinout, and (c) BF998 physical component [24]

Figure 1 (a) depicts the typical device structure of the DG MOSFET. It consists of a top and bottom gate, source, and drain terminals, (b) shows the internal pinout of BF998 DG MOSFET, and (c) has the physical structure of the DG MOSFET. The DG MOSFET can be used in two different modes of operation; in symmetric at this mode, both gates are supplied with the same gate voltage, whereas in asymmetric mode, both gates are independently fed with different sources of supply [22, 25, 48]. The asymmetric mode of operation is susceptible to the Silicon body, which impacts short channel effects; as a result, the symmetric mode of operation will be utilized in this research work.

Table 1. Summary of the advantages and disadvantages of the DG MOSFET

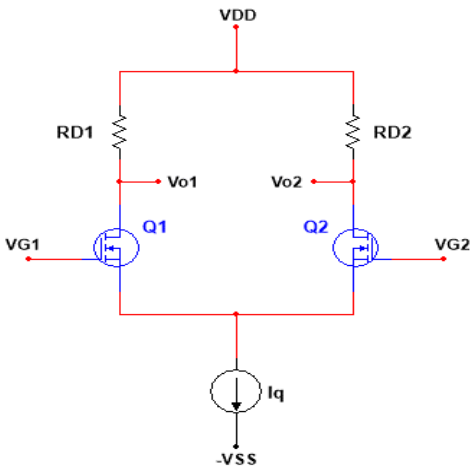
Advantages	Disadvantages
• Higher drive currents at lower supply voltage and threshold voltage. • The channel and gate-leakage current is reduced an off-state to save power. • Isolated power gate control helps to save power and chip surface area. • It has a better sub-threshold slope (approximately *60* mV/decade). • There are no discrete dopant fluctuations. • The energy is a quadratic function of the supply voltage.	• Alignment of both gates with respect to one another. • Source and drain self-alignment to both gates. • The low resistance path is used to connect the two gates.

2.2. Differential Amplifier and Its Operation

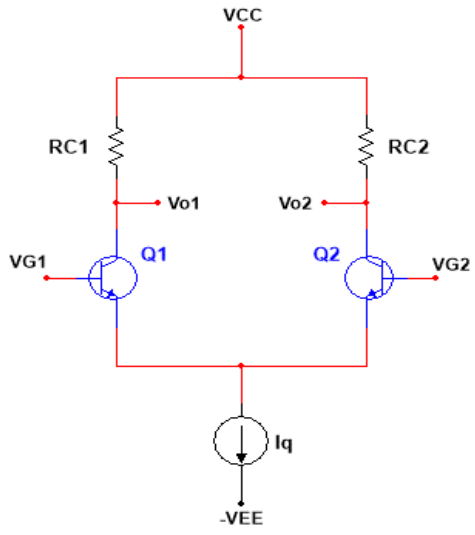
In analog Integrated Circuits (IC), the differential amplifier design has become the most used building block. Every operational amplifier, for example, has a differential amplifier as its input stage [27, 48]. The fundamental differential amplifier design was introduced in the 1940s for use with vacuum tubes and later used discrete bipolar transistors. Ultimately, the development of integrated circuits significantly increased the differential pair's popularity in MOSFET and bipolar technologies [27]. Differential amplifiers are ideal for IC manufacturing for two primary reasons: Firstly, the circuit matching between the two sides of the circuit significantly impacts the differential pair's performance. The manufacture of IC can produce devices with matching specifications that track a broad range of variations in environmental factors. Differential amplifiers naturally require more components than single-ended circuits, nearly twice as many. The second reason is the ability to bias the amplifier and connect amplifier stages without bypass and coupling capacitors, which are required to design discrete-circuit amplifiers.

Figure 2 displays a fundamental differential signal processing method. The benefit of a differential signal is that undesirable noise or harmonics have an equal impact on both signals that make up the differential signal. As a result, harmonics or undesired noise do not impact the differential single-ended output that results. The difference between the signals provides the physical property and is quantified by the differential signal output is A ($V_{in1} - V_{in2}$), where 'A' is the differential gain would be the signal seen at the receiver if V_{in1} and V_{in2} were the operational amplifier's input signals. Each input signal will be similarly affected if a non-ideal signal is added to the differential pair of signals. Any undesirable components, such as noise of any kind, can be effectively minimized by processing the differential between the input signals [28-30].

A differentiable pair of signals are frequently used in situations where the signal source (sensors or other electronic measurement tools) and signal sink (microcontroller or any other different user interface) are separated by a large distance or require precision in the quantifiable measurements taken (e.g., pressure, temperature, humidity, etc.). The MOSFETs or BJTs can be used to construct the differential amplifier, as depicted in Fig. 2. The voltage difference between two inputs (V_{G1} - V_{G2}) is multiplied by some constant factor A_d, the differential gain, in a differential amplifier. It may have a single output or a pair of outputs, with the voltage difference between the two outputs serving as the signal of concern. A differential amplifier will also reject the input signal portion in both input signals ($V_{G1}+V_{G2}$)/2. This is known as the common mode signal [27, 28].



(a)



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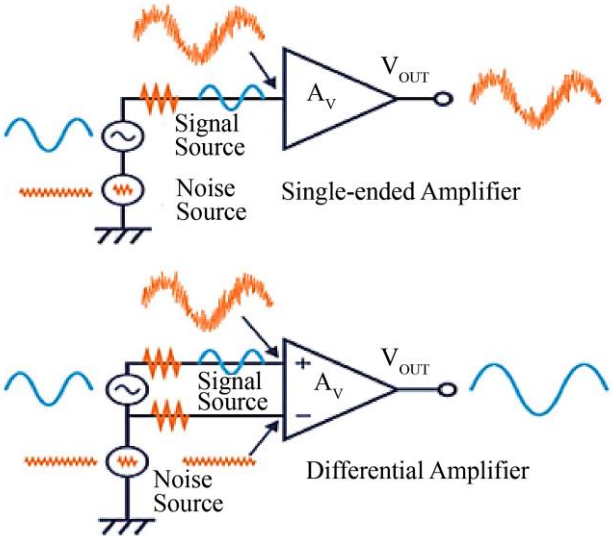


(c)

Fig. 2 (a) MOSFET-based differential amplifier, (b) BJT-based differential amplifier [45], and (c) differential amplifier with a noise source and single output

Figure 2(a) comprises two matched transistors, M_1 and M_2, with their sources connected and biased by a constant-current source (I_q). It is assumed that the current source is ideal and has infinite output resistance. Each drain is connected to the positive source via a resistance (R_D). Active (current source) loads are typically used. However, the fundamentals of the differential-pair operation with simple resistive loads are used [31-33]. Whichever the load, it is critical that the MOSFETs do not enter the triode region of operation [27, 48]. A double-gate-based MOSFET differential amplifier has been designed for this research work and includes the resistive loads.

3. Methodology of System Design of Differential Amplifier using Double-Gate MOSFET

Differential amplifiers are primarily used to reduce noise comprising typical differential and common-mode noise, which could be conveniently reduced with an operational amplifier. Two main factors cause common-mode noise; first, electromagnetic induction and other factors produce noise in the electrical wires and cables, resulting in a potential difference (noise) between the signal source and circuit ground. Secondly, a ground potential rise occurs when current flows into the ground of one circuit from another [34-36]. Noise causes the ground potential to vary in both cases. Common-mode noise is challenging to eliminate with standard filters. To overcome this common mode noise, differential amplifiers are employed.

This research work has designed a differential amplifier circuit using a DG MOSFET. The Silicon n-channel BF998 MOSFET has been chosen for this design because it reduces the Short-Channel Effect (SCE). It is also better than other DG MOSFETs, such as BF904WR, because, according to the datasheet, it is designed to have up to a supply voltage of 12 V for VHF and UHF applications [37]. In contrast, the other can have only up to 7 V, low noise gain at high frequencies, and high forward transfer admittance to input capacitance ratio [38]. The proposed differential amplifier circuit consists of two matched (DG MOSFETs), the same drain resistance (R_1 and R_2), and a current source (made using R_3 and V_1), as can be seen in Fig. 7. However, in this work, a resistor has been used instead of the current source to generate current. The constant tail current source will generate a constant current that will be shared amongst the two matched transistors so that the current through M_1 and M_2 will add to I_T.

The proposed differential amplifier is supplied with a DC voltage of ±12 V. An electronic device simulator has been used to simulate the proposed differential amplifier and to analyze the performance using various parameters. Figure 3 depicts the process used to design the proposed differential amplifier using DG MOSFET. The different blocks summarize the step taken to design. Basic information about a DG MOSFET has been discussed to observe its performance compared to existing Single-Gate (SG) MOSFET. This has been done with background information on differential amplifiers and their basic operation. The last block depicts the analysis of results to observe the performance of the proposed differential amplifier.

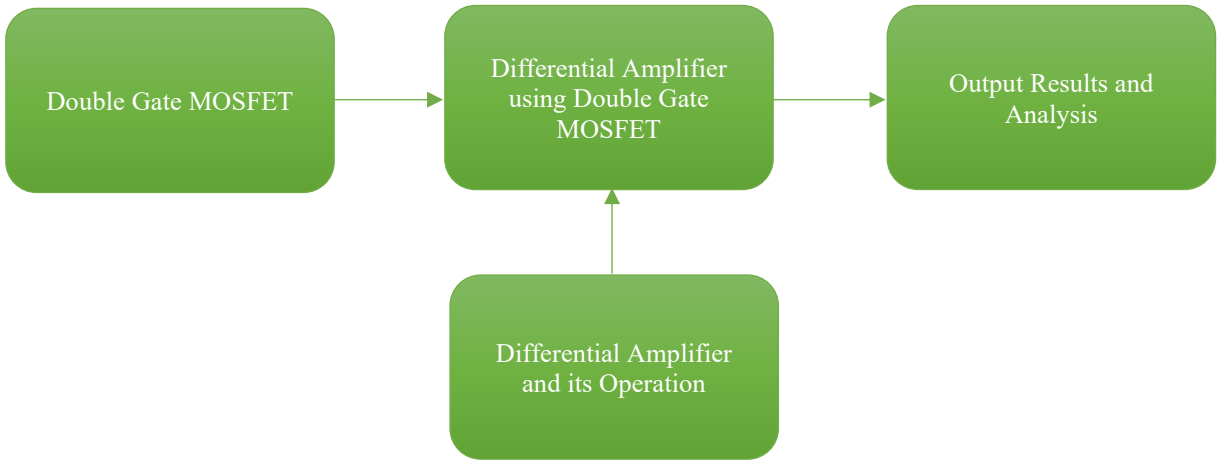
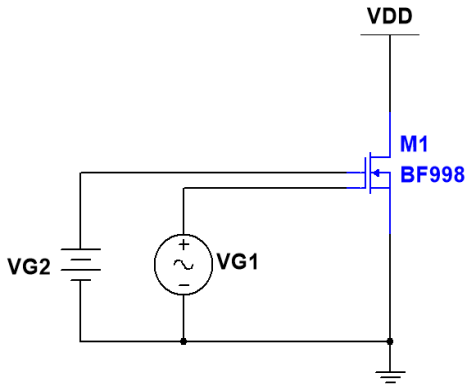


Fig. 3 Design process of a DG MOSFET-based differential amplifier

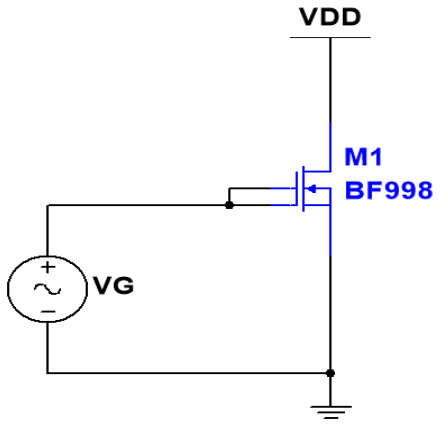
4. Circuit Design of Differential Amplifier using Double-Gate MOSFET

The BF998 MOSFET can be driven independently where both gates have distinct signals and are biased individually and symmetrically where both gates have the same work function or are supplied with the exact signal [24, 39], as illustrated in Fig. 4.

If gates are individually driven, it is advised that gate-1 be supplied with the low frequency and voltage signal and gate-2 be used to bias the MOSFET appropriately. Furthermore, gate-2 is used to bias the MOSFET in a saturation region. Nevertheless, since gate-2 is in charge of the transconductance, threshold voltage, and current characteristics, operating each MOSFET asymmetrically allows much greater control. Fig. 5 depicts the output characteristics of the BF998. Here BF998 MOSFET is in saturation; it is advised that gate-2 be biased with a DC voltage of 4 V. Depending on the drain current, gate-1 voltage may be varied between -0.5 V to 0.5 V.



(a)



(b)

Fig. 4 (a) Symmetrically driven MOSFET, (b) Asymmetrically driven MOSFET

When applied, a change in V_{G2} results in an increased or reduced transconductance. This has been demonstrated by [22], where the device's linear section has a more significant gradient when V_{G2} is increased to 2 V. Therefore, lowering V_{G2} results in a lower voltage at saturation and lower demand for drain current.

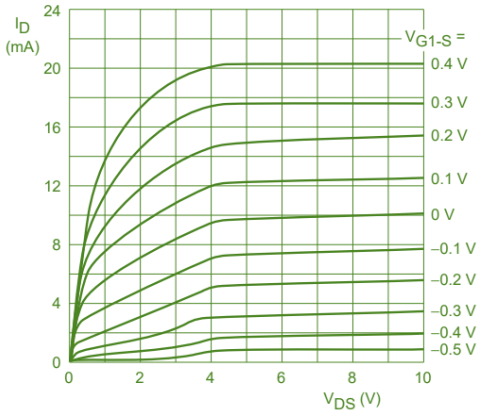


Fig. 5 Drain current vs. drain voltage [27]

The differential amplifier combined with a voltage divider would make up the two primary components of the proposed differential amplifier. Voltage dividers are helpful in providing various voltage levels from a single supply voltage. This common supply could be across a dual supply, such as 5 V or 12 V, or a single supply that is positive or negative, such as +5 V, +12 V, -5 V, or -12 V, etc., with regard to a common point or ground, typically 0 V. A voltage divider will be used to bias gate-2 using the available 12 V supply. Gate-2 will be biased with 5 V from the voltage divider, and the voltage divider is depicted in Fig. 6. The fundamental formula to calculate the required voltage is [49]:

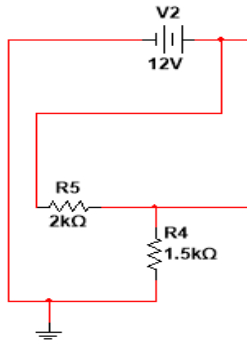


Fig. 6 Typical voltage divider

$$V_o = V_2\left(\frac{R_4}{R_4+R_5}\right) \quad (1)$$

This voltage divider depicted in Figure 6 is important to minimize using different power sources to bias gate-2 on both MOSFETs. The input voltage (V_2) is 12 V, R_4 was calculated to be 1428 Ω (1.5 kΩ is used as a standard value), and R_5 was calculated to be 2 kΩ. The required output voltage of 5 V is obtained. Figure 7 is a complete circuit design of a proposed differential amplifier using DG MOSFET. It consists of two matching MOSFETs(BF998), two same drain resistances, a constant current source, and a voltage divider that is used to bias gate-2 with 5 V to remain in the saturation region. Instead of using an ideal constant current source, the current is generated by inserting a series resistor with a -12 V, V_1 supply. The constant current source is set to have a current of [41]:

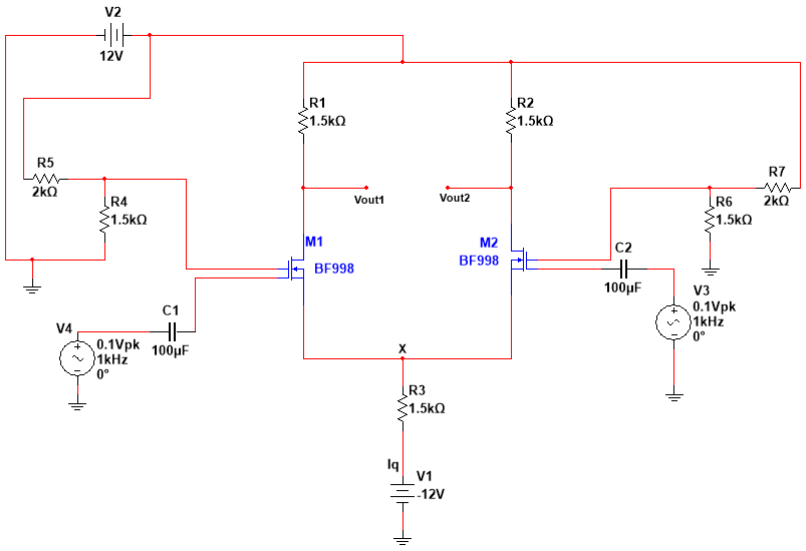


Fig. 7 Designed Double-Gate MOSFET-based differential amplifier circuit

$$I_q = \frac{V_1}{R_3} = \frac{12}{1.5k} = 8mA \quad (2)$$

The circuit contains a dual voltage supply of ±12 V, according to the datasheet of BF998. The gates are fed independently, as seen in Fig. 7. If driven separately; it is suggested that gate-1 should be injected with the RF signal with low frequency and voltage, while gate-2 biases the MOSFET. Furthermore, gate-2 is used to bias the DG MOSFET to generate the necessary drain current [22]. Gate-1 is injected with a 0.1_{pk} AC signal, while gate-2 is biased with a 5 V DC signal for both transistors. Gate-2 is used to turn-ON / as a threshold voltage of the MOSFET. The circuit is perfectly matched.

5. Parametric and Simulated Results Analysis

This section discusses different parameters to evaluate the performance of the realized different amplifier circuit designs and analysis of simulated results. Differential gain, common mode gains, CMMR, and frequency response have been analyzed to evaluate the performance of this amplifier.

5.1. Differential Gain

The differential output signal is directly proportional to the difference between the two input signals in a differential amplifier. That is:

$$V_o \propto (V_4 - V_3) \quad (3)$$

where V_4 is both inputs of the first DG MOSFETs, and V_3 is both inputs of the second DG MOSFET, and V_o is the differential output between the two MOSFETs. The differential gain can be measured with either a differential or a single-ended output. The difference between two signals is amplified and sent to the output. The differential gain is the proportion of the output signal to the input signal. This concept has been represented by [22]:

$$A_d = \frac{V_o}{(V_4 - V_3)} \quad (4)$$

where V_o, V_4, and V_3 are the output voltage, input sign (transistor 1), and input voltage signal (transistor 2). These concepts have been used to calculate the voltage gain in the following sections, B and C when the circuit is operated with single input - single output and single input - differential output.

5.2. Single-Input with Single-Output

Figure 8 depicts a proposed DG MOSFET single input with single output differential amplifier. A single device (M_1) is used, and the second transistor (M_2) input terminals are grounded. The single output is taken on the drain terminal of M_2, represented by $V_{out.}$

The capacitor in series with the AC signal source (on gate-1) filters out any DC component. Gate-2 is biased is 5 V from the voltage divider. The current flowing through M_1 increases when the input signal (on V_4) becomes positive. At point X, this increased current results in a positive-cycle signal. The source of M_2 sees the inverted signal. Since the base of M_2 is grounded, a positive-cycle signal on the source terminal of M_2 causes the current to decrease and, eventually the voltage across R_2 to drop. As a result, the voltage on the drain terminal of M_2 increases (input signal is amplified). The current flowing through M_1 decreases as the input signal becomes negative—this decrease in current at point X results in a negative-cycle signal on the source terminal of M_2. The current flowing through M_2 increases as the source of M_2 becomes negative. More voltage is dropped across R_2 because of the higher current. As a result, , the voltage at the drain of M_2 drops, and the output terminal (V_{out}) experiences a negative cycle signal.

Figure 9 depicts the single input – single output signal. The input signal has an amplitude of 0.1 $V_{pk\ -\ pk}$ at a frequency of 1 kHz. The output signal of the amplifier was measured to be 1.36 $V_{pk\ -\ pk}$. The gain of this setup is -6.8 V/V. Although this differential amplifier provides amplification of AC or DC signals, the capabilities of a differential amplifier are not fully exploited. Table 1 summarizes the results and the behavior of this circuit setup when the amplitude of the AC input signal is varied.

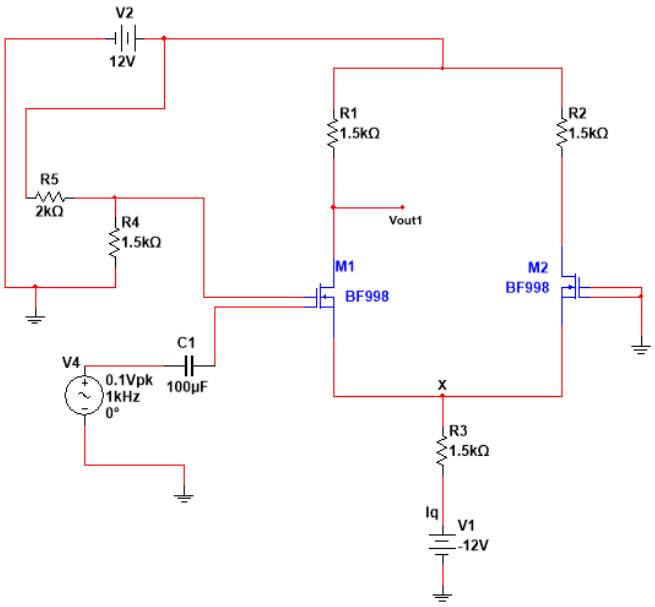


Fig. 8 Single input – Single output differential amplifier

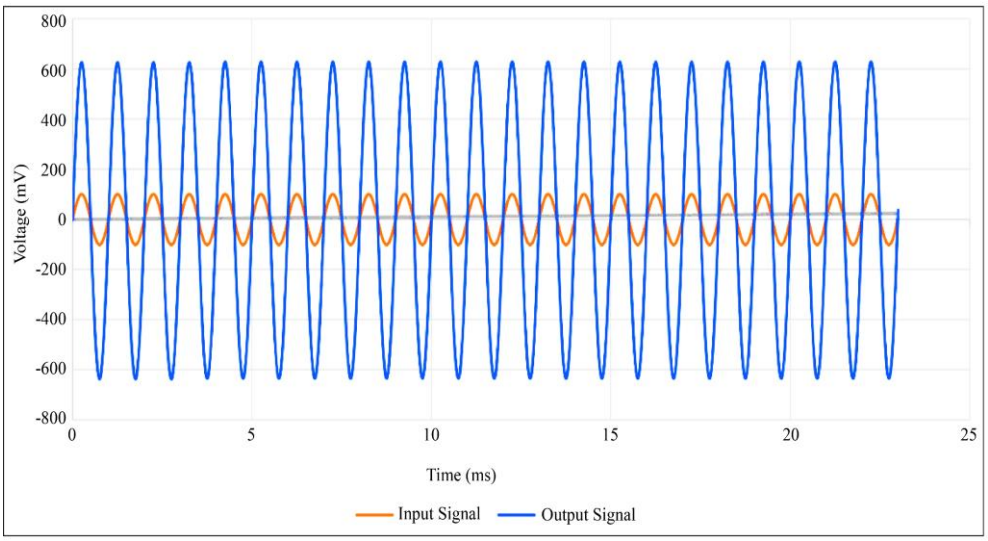


Fig. 9 Single input – single output signal

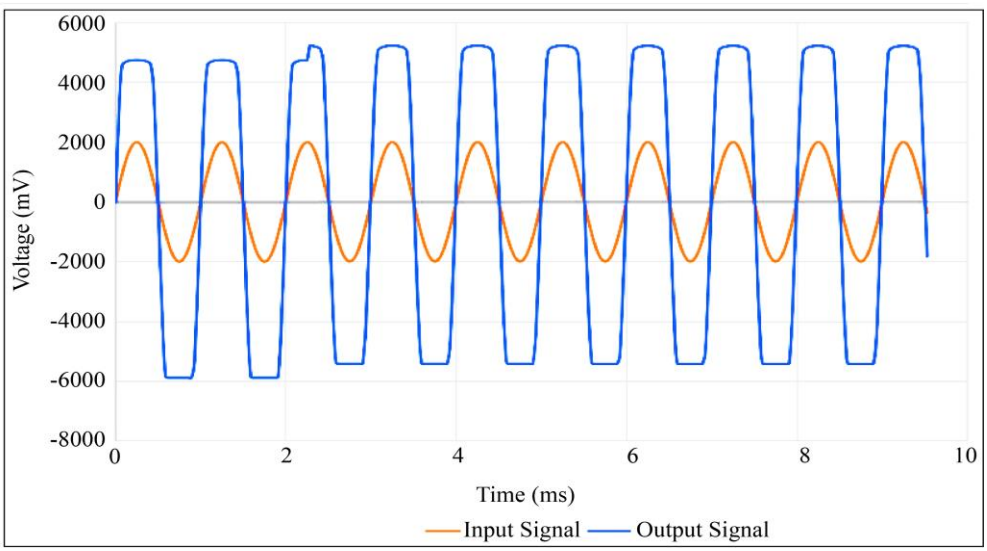


Fig. 10 Distorted output signal with the AC input signal (V_4) amplitude of *1 V*

Table 2. Single input – single output results for different values of V_4

MOSFET-1 (V_{G2})	MOSFET-1 (V_4; V_{pk})	MOSFET-2 (V_G; input)	Single Output Signal (V_{pk-pk})
5V	0.1	0V	1.36
5V	0.3	0V	4.03
5V	0.5	0V	6.59
5V	0.8	0V	10.00

As the amplitude of the input signal varied from 0.1 V_{pk} to 0.8 V_{pk}, the output signal was distorted from the values above 0.5 V_{pk}. This means that the proposed differential amplifier can work as a single input and single output amplifier with an amplitude from 0.1 V_{pk} to 0.5 V_{pk}, with the highest gain at 0.1 V_{pk}. This can be seen in Fig. 10. This is because the MOSFET is no longer in the saturation region, and the gate-1 voltage is above the required value.

5.3. Single-Input with Differential-Output

A designed DG MOSFET-based single input-differential output differential amplifier is depicted in Fig. 11. The differential output signal is taken between the drains of M_1 and M_2, denoted as V_{out1} and V_{out2}. The operation of this circuit is identical to that of the previously discussed single input – single output differential amplifier, except that on this one, the output is taken differentially (difference between two outputs). When the input signal on gate-1 (V_4) rises, the source terminal of M_1 experiences this signal, and on the source terminal of M_2, the signal is inverted. This results in the output signal on the drain of M_2 being in phase while the signal is out of phase on the drain terminal of M_1 from the original input signal.

A differential amplifier can produce two amplified differential output signals from a single-input signal. The fact that the combined output signal from outputs one and two will have twice the amplitude of the separate outputs makes this setup beneficial. In other words, measuring the output signal across the two output terminals can increase the gain of the differential amplifier by a factor of two. The input signal and this single-output signal will be in phase. Figure 12 depicts the results from the circuit design, single input–differential output signal at 1 kHz. The input signal has an amplitude of 0.1 V_{pk-pk} at 1 kHz. The output signal of the amplifier has been simulated to be 2.62 V_{pk-pk}. The gain of this setup is calculated to be -13.10 V/V. Based on the results, it can be seen that taking a differential output doubles the gain of the amplifier. Table 2 summarizes the results and the behavior of this circuit setup when the amplitude of the AC input signal is varied.

Varying the signal's amplitude from 0.1 V to 1 V yields the plotted graph. This circuit behaves in the same way as the previously discussed circuit above 0.5 V. It can be observed that the signal is clipped when the amplitude is above 0.5 V.

5.4. Common Mode Voltage Gain

The amplification given to signals appearing on both inputs of the transistors relative to the common ground is referred to as common-mode voltage gain. Since a differential amplifier is intended to amplify the difference between the two voltage signals applied to the inputs of the transistors, the common mode voltage gain can be measured using the differential output voltage. Consider applying equal voltages to the inputs of the transistors, as depicted in Fig. 14.

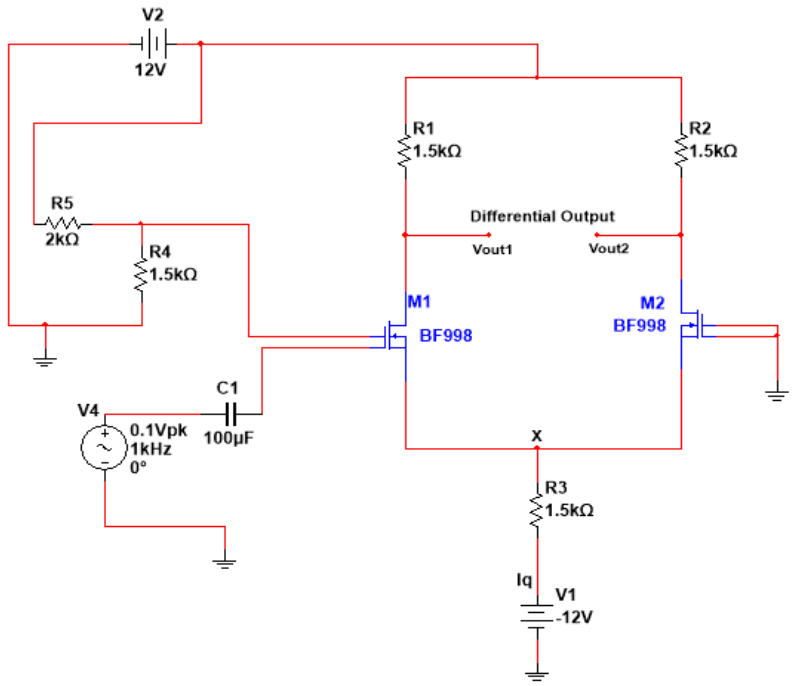


Fig. 11 Single input – differential output circuit diagram

The ideal result would be zero voltage at the output, but this is unrealistic. This is because the MOSFETs and resistors will not perfectly match in a practical situation. Whereas in simulation, the devices are assumed to match perfectly. A common mode signal can be developed by connecting the gate terminals of transistors M_1 and M_2, then attaching the connected terminals to a common voltage source. As can be seen in Fig. 14, gate-1 of M_1 is connected to gate-1 of M_2. This is the same as for gate-2. In ref. [44], modeling of a small signal common mode signal has been done, and the derivation change in drain resistance. This mismatch will eventually affect the output voltage on both output sides of the differential amplifier. This means the differential amplifier will amplify that difference voltage sensed at the output.

Table 3. Single input – differential output simulated results for different amplitude values on M_1

MOSFET-1 (V_{G2})	MOSFET-1 (V_4, V_{pk})	MOSFET-2 ($V_{G,\ input}$)	Differential Output Signal ($V_{pk\text{-}pk}$)
5V	0.1	0V	2.62
5V	0.3	0V	7.80
5V	0.5	0V	12.70
5V	0.8	0V	19.30

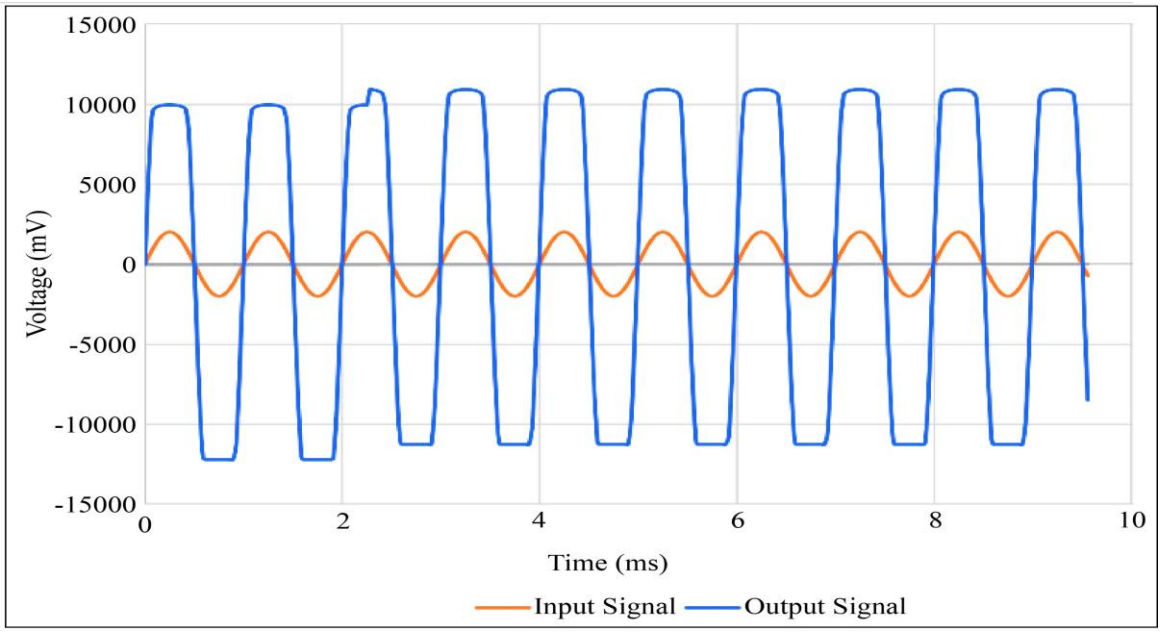


Fig. 12 Single input – differential output signal

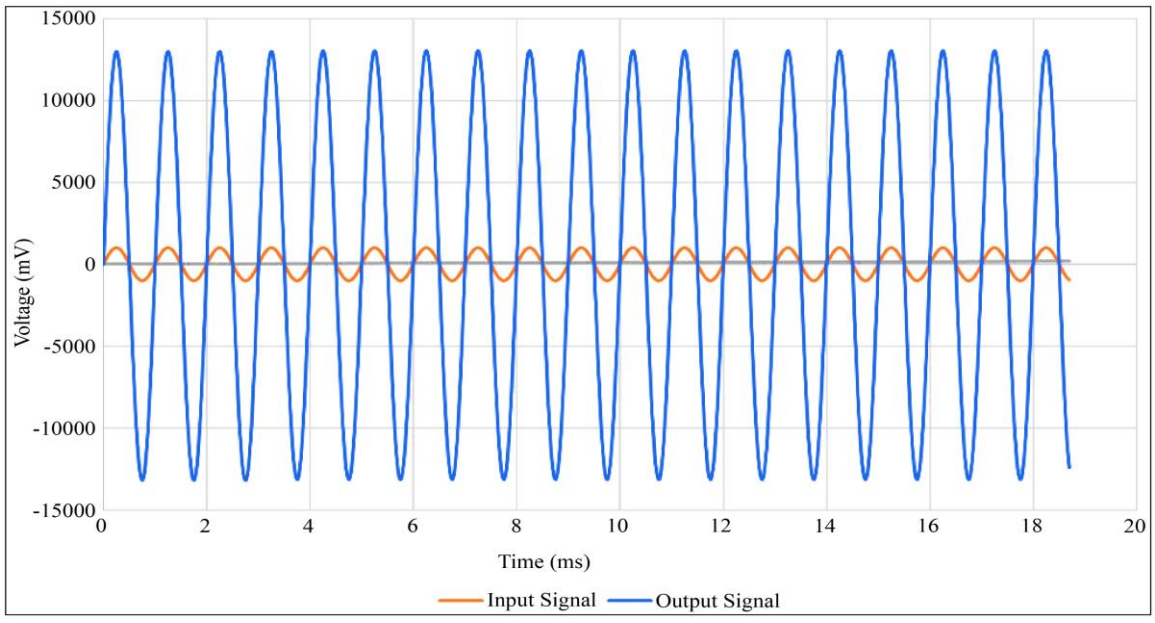


Fig. 13 Distorted output signal with the AC input signal amplitude of *1V*

The drain resistance of M_1 is R_{D1}, and for M_2 is $R_{D2} + \Delta R_{D2}$. This results in different output voltages. The common mode voltage gain without taking into consideration the mismatch is [42]:

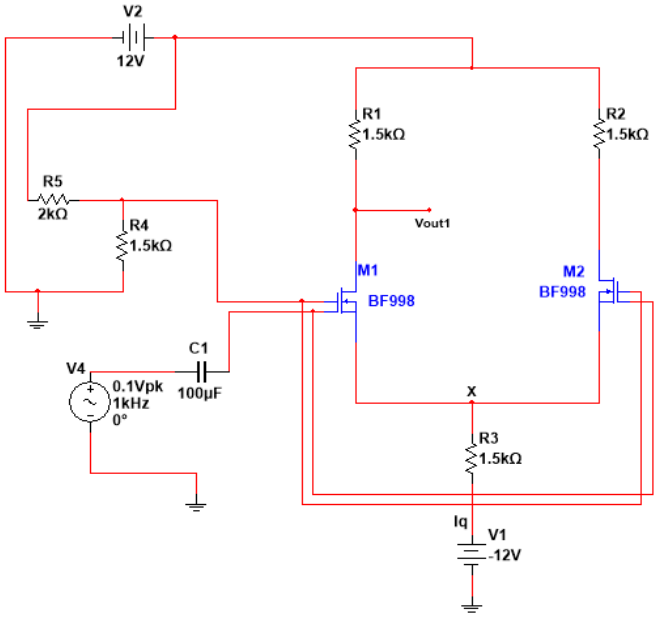


Fig. 14 Common-mode input voltage circuit diagram

$$A_{v(cm)} = -\left(\frac{\Delta R_A}{2R_3}\right) \quad (5)$$

And the common mode voltage gain with mismatch is:

$$A_{v(cm)} = -\left(\frac{\Delta R_A}{2R_{SS}}\right)\left(\frac{\Delta R_A}{R_A}\right) \quad (6)$$

where ΔR_A represents a mismatch in drain resistance. Figure 15 depicts the differential output signal of the common mode input signal.

To cater for the mismatch, R_{D2} has been changed to 1.499 kΩ instead of 1.50 kΩ to observe the behavior of the common mode input voltage – differential output voltage signal. The differential output voltage has been obtained as 39 µV with the common mode input voltage of 0.1 V_{pk}, and the common mode output voltage gain has been obtained as 180 µV/V, and this is ideally zero.

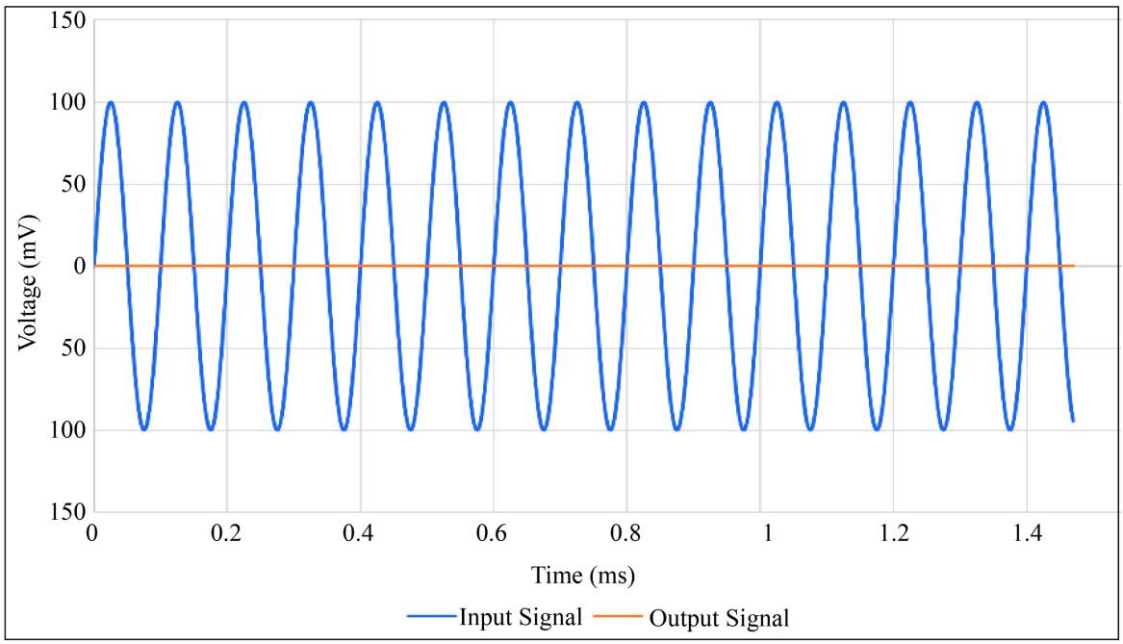


Fig. 15 Differential output voltage signal with common mode input (DG MOSFET)

5.5. Common Mode Rejection Ratio (CMMR)

The CMRR measures a differential amplifier's capacity to reduce signals shared by both inputs. The ideal differential amplifier has a very high gain (single-ended or differential) and no gain for common-mode signals [23, 45, 46]. It is the magnitude of its differential gain. $|A_d|$ divided by the magnitude of its common-mode gain $|A_{(cm)}|$ [22,23] as:

$$CMRR \cong \frac{|A_d|}{|A_{(cm)}|} \tag{7}$$

and is normally expressed in dB,

$$CMRR(dB) \cong 20\,log\left(\frac{|A_d|}{|A_{(cm)}|}\right) \tag{8}$$

The common mode rejection ratio for single input – single output and single input – differential output voltage are 34.87 kV/V (90.85 dB) and 67.18 kV/V (96.54 dB), respectively.

5.6. Frequency Response

The frequency response of an electronic circuit allows one to observe precisely how the output gain and phase change at a single frequency or over a wide range of frequencies ranging from 1 Hz to ± 100 MHz. Obviously, it depends on the circuit's design requirements. The amplifier will not perform adequately above a certain cut-off frequency. Concerning Eq. 6, the frequency response can be calculated as follows [23, 45, 46]:

$$f = \frac{1}{2\pi C_T R_{DS}} = \frac{1}{2\pi\tau} \tag{9}$$

Where τ as a time constant.

Figure 16 depicts the frequency response of the single input – single output differential amplifier using double gate MOSFET. The designed DG MOSFET-based differential amplifier, cut-off frequency for single input – single output, and gain magnitude have been obtained as 30 MHz and 17 dB, respectively.

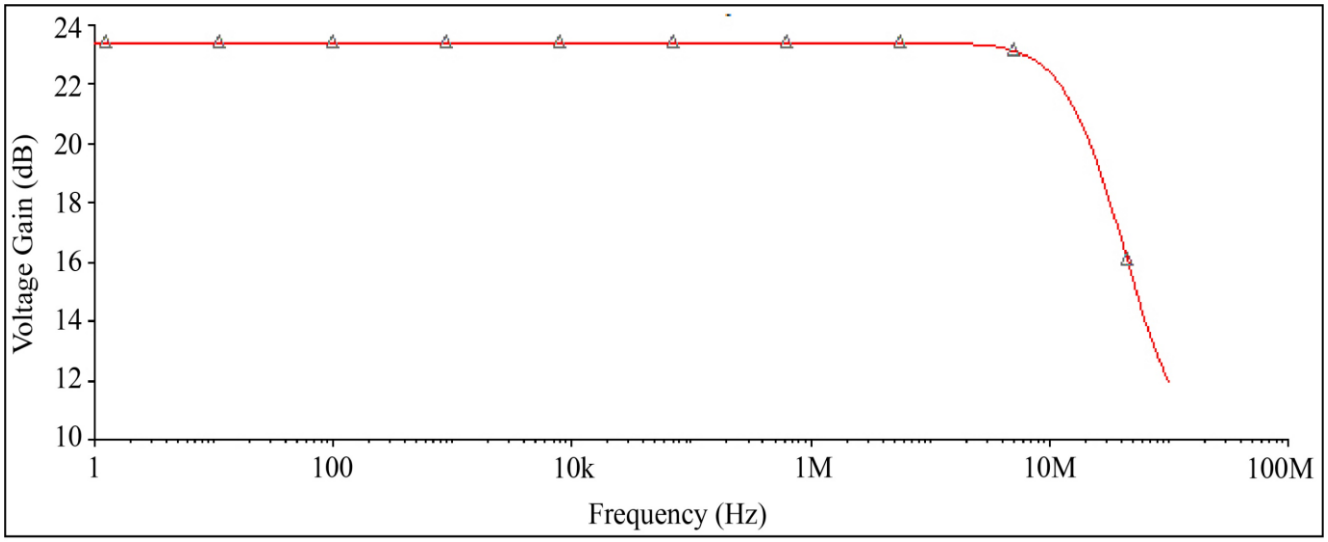


Fig. 16 Frequency response for single input – single output frequency response

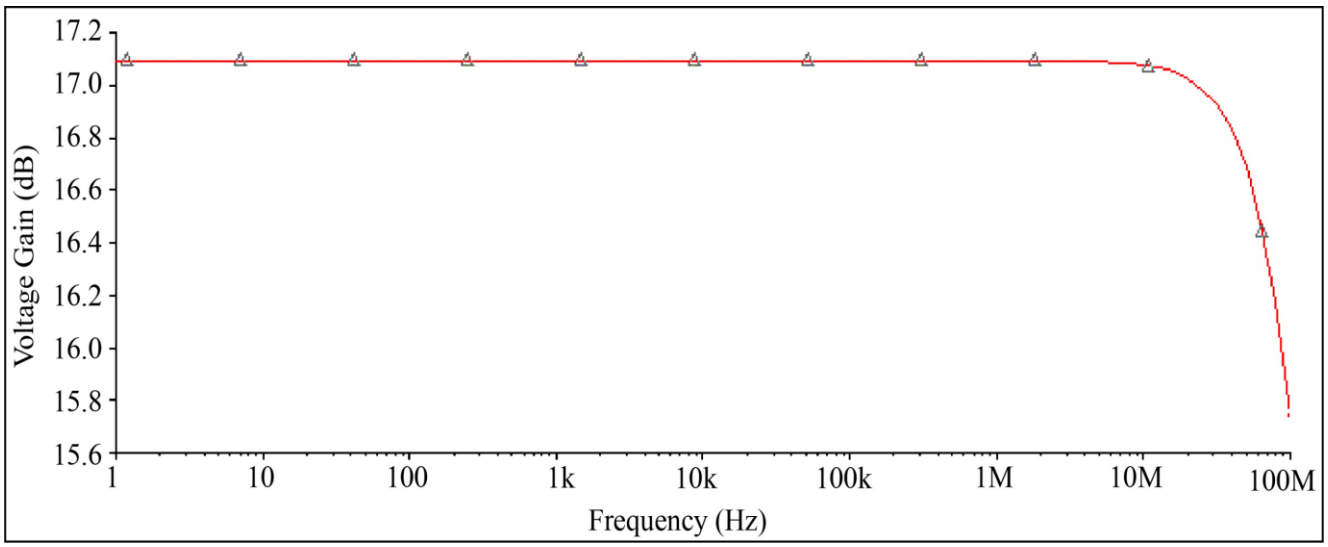


Fig. 17 Frequency response for single input – differential output frequency response

Table 4. Comparative analysis of the designed differential amplifier using DG MOSFET with existing models

References	Device	Gain (dB)	Common mode gain (V/V)	CMRR (dB)	Cut-off frequency (kHz)
[18]	DG MOSFET	18.8	32×10^{-3}	19.06	29000
[19]	DG MOSFET	4.6-5.1	$84.62\times10^{-6} – 3.7\times10^{-3}$	>75	42000
[41]	SG MOSFET	18	-	11.34	0.0987
[42]	SG MOSFET	70	-	72	30000
[43]	SG MOSFET	50	-	-	200
[44]	SG MOSFET	59	-	-	-
This work	DG MOSFET	22.3	39×10^{-6}	96.54	60000

The cut-off frequency for single input–differential output was 60.167 MHz with a gain magnitude of 23.4 dB. Figure 17 depicts the frequency response of the single input–differential output differential amplifier using double gate MOSFET has a wide bandwidth. It will be able to accommodate or be used in different applications. A comparative analysis of various parameters has been summarized in Table 4. The results show that the proposed differential amplifier outperforms the existing designs, especially for the gain and frequency response.

5.7. Comparative Analysis

The aforementioned comparisons can be adapted from [22,23], which includes a design and comparative analysis of active and resistive loaded differential amplifiers using double-gate MOSFET. Further comparative analysis with existing designs that used single-gate MOSFETs has been done. Table 4 contains a list of them.

Based on the comparison in Table 4, it can be observed that the proposed design of the differential amplifier proves to outperform the already existing models/designs with respect to voltage gain, CMRR, and cut-off frequency. The performance of the proposed differential amplifier also proves that the two gates of BF998 create two in-series capacitors at which, if one adds them, the capacitance of the two in-series capacitors becomes less compared to one capacitor. This reduces the short channel effect and gate current leakage on the device, eventually improving its performance.

6. Conclusion and Future Recommendations

The design of a differential amplifier using the DG MOSFET was analyzed in this work. The basic operation of the DG MOSFET and differential amplifier was discussed and assisted in designing the proposed amplifier. The BF998 DG MOSFET was used to design the proposed differential amplifier. The amplifier's performance was analyzed using parameters such as single input – single out the gain, single input differential output voltage gain, common-mode input gain, CMRR, and frequency response. These were realized as: -6.8 V/V, -13.1 V/V, 39 μV, 34.87 kV/V (90.85 dB), 67.18 kV/V (96.54 dB), and 60 MHz, respectively. These results prove that the amplifier performs well, and using the DG MOSFET in independent mode yields improved results.

In future, a current source can be used to design a reliable constant current source using transistors to avoid high voltage drop across the resistor. This is believed that it can also improve the performance of the differential amplifier in terms of differential gain and CMMR. In addition, this Silicon-based DG MOSFET can be replaced with high-k dielectric materials, such as HfO_2, Al_2O_3 etc. After further improvement, this DG MOSFET can be replaced with the Cylindrical Surrounding Double-Gate (CSDG) MOSFET [47].

Statements & Author's Declarations

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Author Contributions

Thabiso Tekisi (TT) and Viranjay M. Srivastava (VMS) conducted this research; TT designed and analyzed the model with data and wrote this article; VMS has verified the result with the developed model; all authors approved the final version.

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