International Journal of Engineering Trends and Technology
ISSN: 2231 – 5381 / https://doi.org/10.14445/22315381/IJETT-V71I2P230

Volume 71 Issue 2, 268-280, February 2023


*Original Article*

# Prototype Design of Double-Pole Four-Throw RF Switch Using Dual-Gate MOSFET

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Received: 23 November 2022 Revised: 14 January 2023 Accepted: 14 February 2023 Published: 25 February 2023

***Abstract*** *- This research work designs a Double-Pole Four-Throw (DP4T) switch using Dual-Gate (DG) MOSFET, which can be used in electronic and communication devices at the Micro- and Nanotechnology levels. Multiple recourses have been reviewed to identify the feasibility of the switch. Thereafter, DG MOSFET was selected due to its minimal impurity scattering, high current drive, and better control of short-channel effects compared to Diodes, BJTs, and other traditional MOSFETs. The switch has been compared to an alternative switch topology. Reasons based on the research have been stated to legitimize the switch's effectiveness over SPST, SPDT, DPDT, etc. configurations. This device has been fabricated and tested for various parameters such as differential mode gain, common mode gain, and frequency response. The testing process resulted in differential mode gain (3.58 dB and 3.70 dB), common mode gain (2.72 dB and 2.73 dB), and isolation gain (70 dB and 60 dB) for 50 MHz and 100 MHz, respectively. The focus of the work is the design of the switch based on mathematical analysis and approximations.*

***Keywords*** *- Dual-gate MOSFET, Efficiency, Switch, Microelectronics, Nanotechnology, VLSI.*

## 1. Introduction

The communication system is a technology that conveys information from one location to another. There is a vast extent of different kinds of applications of information transceiver systems that are used. Thus, different types of communication system technology have developed over the years since the discovery of Radio Frequency (RF) and electromagnetic waves [1, 2]. Typical devices or systems contain numerous parts, components, or even a range of devices based on technology, varies from electric circuits, electronics, microprocessors, electromagnetics, communication networks, and signal processing, to mention a few fields in the communication system [3-5,34]. The improvement in technology and the endeavor for advanced convenience led to more useful and sophisticated wireless communication technology; these range from satellite communication, broadcast radio, infrared communication, microwave communication, mobile communication systems, Bluetooth technologies, Wi-Fi technologies, etc. [6-8]. In electronics, information is recognized and processed differently depending on the system. For example, information at one point in time could be digital, analog, or modulated propagating waves [9, 10]. Analog systems process continuous signals and digital systems process discrete information; methods and strategies have been developed to convert and interpret one to the other [11-13,24]. These communication systems have had significant challenges over the years, such as security, secrecy, privacy, resource and spectrum utilization, energy efficiency enhancement, integration of wireless information, power transfer, modulation, resource and interference management, wireless access techniques, transmission speed, etc.

Another major challenge in communications is switching. One of the earliest switching systems was analog switches, where an operator had to receive a request and direct the communication line to the appropriate location [14, 15]. As technology advanced in antennas and nano- or micro-processing technology, analog switches were replaced with automatic analog and digital switches. This research work is based on analyzing and developing a basic RF switch. The basic functionality is sending the signal to the antenna through a switching system after signal modulation or processing. After receiving a signal from the antenna, the signal travels through a switching system to processors. RF switches can create multiple pathways for the signal using a switch. One antenna can be used as both a transmitter and a receiver. Depending on the developers' specifications, more than two pathways can be alternated with reference to one antenna [16, 17]. Figure 1 shows a basic block diagram of a system with two antennas and four pathways – this kind of switch configuration is referred to as Double-Pole Four-Throw (DP4T) configuration. The basic DP4T switch integrates a system that receives RF signals from one antenna and transmits them to one antenna. The RF1 transmits or receives the signal from TX1 and RX1, respectively, and these are switched with the control input at PORT-1.

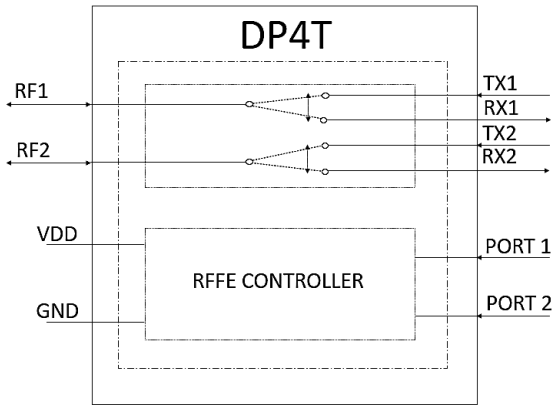



**Fig. 1 High-level design of DP4T switch**

The same applies to RF2, which corresponds to TX2 and RX2 and is controlled by input at PORT-2. This RF switch is based on DG MOSFET for the RF regime, and the control of the switch is based on an NPN transistor.

The overall system comprises four DG MOSFETs, two configured for transmission and the other for receiving. The DP4T switch in double SPDT; each of these SPDT can be divided into two units (for transmitting and receiving) [18, 19]. Single-Pole Single-Throw (SPST) switch is a basis for these; it can only connect one pole to one throw at each time. A Single-Pole Double-Throw (SPDT) switch has one pole, which can be switched to either two paths, whereas Double-Pole Double-Throw (DPDT) has two poles and two paths. An advanced DP4T is suitable for working on a two-antenna configuration while relaying the signal to/from four paths [20-23].

Traditional DP4T switches use MOSFETs as a cell on the main device, requiring up to 5 V high voltage level for control voltage. This would require the antenna to have a large resistance to detect the incoming signals at the receivers. This is unsuitable for modern devices whose proportional size is small and requires low power consumption. Research shows that switches employed using the CMOS technology improve the functionality w.r.t. many of the issues observed in traditional switches, e.g. high-density and cost-efficient. Recent CMOS switches use the Silicon-On-Insulator (SOI) technique, which prevails in high-speed performance, scalability, effective potential, and low power consumption. This architecture is more flexible than bulk silicon substrate due to the buried oxide and thickness of the film, back-gate bias, and substrate doping, which are very important for scaling and optimization. The thin films of this semiconductor are for DG MOSFET, which implements the concept of volume inversion. Due to the incidence of quantum effects, the threshold voltage gradually increases. It is said that a small discontinuity can be observed around the second gate with zero. Research shows a noticeable improvement from Single-Gate (SG) to Dual-gate (DG) MOSFET in terms of improved cross-correlation of the drain and gate current [48]. These MOSFETs can be used with various dielectric materials, but in this work, authors have concentrated on $SiO_2$-based MOSFETs [25, 26].

*Sharma and Bucher* [27] have analyzed the Analog/RF performance of DG MOSFETs in the sub-20 nm regime using the ATLAS device simulator. It was shown that graded channel dual material double-gate achieves higher drain current, peak transconductance, and higher values of cut-off frequency at lower drain currents. Incorporation of a commercially available Single-Pole Four-Throw (SP4T) switch for beam steerable square loop antenna over hybrid was presented by *Deo et al.* [28]. Using this switch with the appropriate selection of its 1:4 output port, a tilted antenna beam can be electronically steered in all four space quadrants. *Lin* [29] has researched an ultra-wideband RF MEMS SP4T switch with four shunt-configured, resistive-contact MEMS cantilever switches. Detailed design and synthesis procedures were provided. It shows that an insertion loss is less than 0.8 dB, the return loss of every route is better than 24 dB, and the minimum isolation is less than 40 dB over the entire band of 1 GHz – 5 GHz. This SP4T switch was actuated by a DC voltage of 35 V - 45 V with little current. *Jung and Kenneth* [30] have demonstrated a one-pole four-throw switch (that can be used to switch between the band select filters of four cellular bands and a single input programmable low noise amplifier) in a 0.18-μm CMOS process.

*Heston et al.* [31] Monolithic GaAs PIN diode single-pole, two-, three-, and four-throw switches provide low noise-figure and insertion loss performance over a two-decade+one-octave bandwidth. From 100 MHz to 20 GHz, the measured noise figure and insertion loss for the three switch types are less than 1 Db through the path, with greater than 45 dB of isolation in the OFF paths. *Beziuk et al.* [32] have designed and fabricated an active four-port microwave switching network embedded into a multi-layer aerospace composite structure. The multifunctional design is based on three broadband integrated device technology Single-Pole Double-Throw (SP2T) RF switches and includes a control and power supply circuit.

*Lee et al.* [33] have developed a Single-Pole Six-Throw (SP6T) antenna switch using metal-contact RF micro-electro-mechanical system (MEMS) series switches for multi-band applications. The fabricated metal-contact MEMS switch with a broad signal line gap of 140 /spl mu/m shows a very high isolation loss of -51 dB at 2 GHz because its centre wedge can control a membrane stiction problem due to the anchor role. *Pranonsatit et al.* [47] have designed, fabricated, and measured the performance of a novel Single-Pole Eight-Throw (SP8T) RF MEMS rotary switch. The average contact resistance of 2.5 Ω was recorded; however, values as low as 1.0 Ω were also found. Worst-case off-state isolation of 31 dB was also measured over the 20 GHz bandwidth.

*Pillay and Srivastava* [5] have realized the dual-gate MOSFET-based source follower. In continuation of that work, this present proposed solution is to design the DP4T RF switch using DG MOSFET. Research has shown that these can easily be scaled down and that the additional gate improves the control of the current that flows through the induced channel. The objective of this work is to design a prototype of the high-frequency operating switch using DG MOSFET. The topology attribute of the switch would constitute a high performance, high efficiency, low power consumption, and low-cost RF switching system device. This work analyses the parameters in RF switching systems. These are Insertion Loss, which measures the ratio of output to the input; Switch Isolation, which is defined as how much of the OFF-state can affect the ON-state operations; Switch Linearity, which is how linear the relation of insertion loss to insertion loss all the frequencies within the required band. This paper has been organized as follows. Section 2 shows the design methodology. System parameter analysis has been done in Section 3. Section 4 describes the designed switch with parametric analysis. Section 5 has the prototype design and its validation. Finally, Section 6 concludes the work and recommends the future aspect.

## 2. Design Methodology of DP4T RF Switch

The selected DG MOSFET for the design is BF909, which is specially designed for operation at a 5 V supply, as shown in Fig. 2 [35-37]. The BF909 Dual-Gate MOSFET is an enhancement-type transistor requiring a positive voltage input to conduct. The MOSFET has high forward transfer admittance and short channel transfer with high forward transfer admittance to input capacitance ratio. The BF909 has a low noise gain amplifier for frequencies up to 1 GHz. The MOSFET is suitable for Very High Frequency (VHF) and Ultra High Frequencies (UHF) applications with voltage supplies between 3 V to 7 V. The proposed DP4T switch is an extended form of the SPDT switch. Each SPDT switch is bidirectional (switched from receiver to transmitter and vice versa).

When the input signal is applied in the transmitting unit, it goes through a DC coupling capacitor to filter out any of the low frequencies [38]. The capacitor acts as an open circuit for lower frequencies since the capacitor would take time to charge while losing the charge when the signal goes negative. The gate input is mostly used for control; this is one of the intriguing features of the DG MOSFET since it allows the insertion of a signal at one gate and controls the output with the other gate. Gate-2, unlike gate-1, is biased and coupled with a capacitor and resistor. The capacitor will realize frequency fluctuations due to the signal input. Thus, if the voltage ripple is too low, the voltage from the selector will mostly drop across the capacitor. The NOT gate provides a solution to control the transmission and reception turns without too many input controls. When the voltage at the control is low, gate-2 will also see a low voltage, thus causing a very low drain current, and the signal will not be transmitted. The NOT gate will then negate that voltage and set a high voltage to the receiver side, and the signal can be received [39-41].

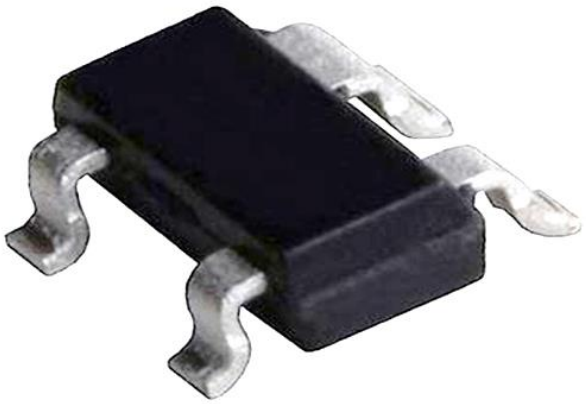


**Fig. 2 The BF909 chip**

The voltage fluctuations at the gates control the drain current, allowing control of the current flows through the resonator. The resonator circuit is designed to have a resonant frequency for the specified frequencies (50 MHz – 100 MHz). This will allow the frequency change caused by the drain current to be reflected in the output. A high pass filter is then used to clip any DC voltage changes at the out, such that the cut-off frequency has to be slightly lower than 50 MHz.

The signal's amplitude or peak voltage must be stepped down at the input to accommodate insertion through the double gate MOSFET. The signal will get clipped at the lower parts if the amplitude is too high. Transmitter has lower resistance to reduce the signal loss, and at the receiver, the resistance is higher to capture the mist of the signal. This process is replicated four times to make a complete DP4T switch. The outputs of the NOT gates are connected to their respective gate-2 biasing circuits on both sections. Finally, the complete system has eight external terminals: two control inputs, ground and supply, two RF inputs for transmitting, two RF outputs for receiving, and two RF input/outputs, which is common for both receiving and transmitting.

## 3. System Parameters Analysis

Various parameters have been analyzed for their functionality, such as insertion loss, isolation, power handling, Linearity, switching time, and reflection coefficients. Both gates are biased because they are not using more than 3 V from the supply [42,49]. This means the input signal must be less than 3 V peak voltage. Therefore, the values provided in the datasheet have been used to design a system based on DG MOSFET. A point of note is that the datasheet includes the information for drain-source voltage of 5 V. Since the system will be using 3 V, some of the estimated values might be slightly smaller or different in the analysis.

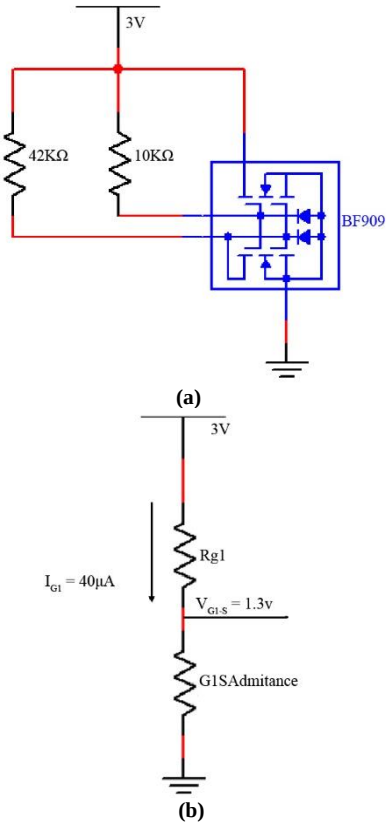



**Fig. 3 (a) Gate-1 and gate-2 biasing basic circuit, and (b) Estimation of $R_{G1}$.**

Figure 3 shows the system will use one voltage ($V_{DS}$) equal to $V_{GG}$ = *3 V*. The function clearly shows that the highest current at $V_{GG}$ = *3 V* is at $R_{G1}$ = *47* Ω. At this point, the current is approximately *17.5 mA*. To get a higher drain current, the datasheet shows that the drain current of 30 mA can be obtained when $V_{G1\text{-}S}$ = *1.4 V* and at $V_{DS}$ = *3 V*, the current is approximately 27 mA. The gate resistances have been calculated as follows:

$$R_{G1} = \frac{Vcc - V_{G1-S}}{I_{G1}} = \frac{3 - 1.5}{60x10^{-6}} = 25\ k\Omega \quad (1)$$

$$R_{G1} = \frac{Vcc - V_{G1-S}}{I_{G1}} = \frac{3 - 1.3}{40x10^{-6}} = 42.5k\Omega \cong 47\ k\Omega \quad (2)$$

Since 47 kΩ gives more drain current, this turns out to be $V_{G1-S} =$ 1.3v with the gate-1 current of 40 µA. The current that flows through gate-2 is very small; therefore, all the current from the supply drops to the gate, and in this case, $V_{G2} =$ 3v. According to the datasheet, since 1.3 V has been selected as gate-1 voltage, with $V_{DS} = V_{G2} =$ 3, the estimated drain current is 22.5 mA.

The input port or the RF connector is estimated to have a resistance of 50 Ω [42, 43]. A DC coupling high pass capacitor is placed at the input to filter DC currents. With a shunt resistance of 50 Ω and capacitance for the cut-off frequency of 500 kHz is calculated as C = 6.4 nF. The supply at gate-2 needs to be as DC as possible; the change in gate-1 voltage causes some current ripples at gate-2. Since the cap at the input filter has lower frequencies, the cap at the gate filter has higher frequencies. For this, the same capacitor is used as a low-pass filter. Figure 4 shows the full input side configuration.

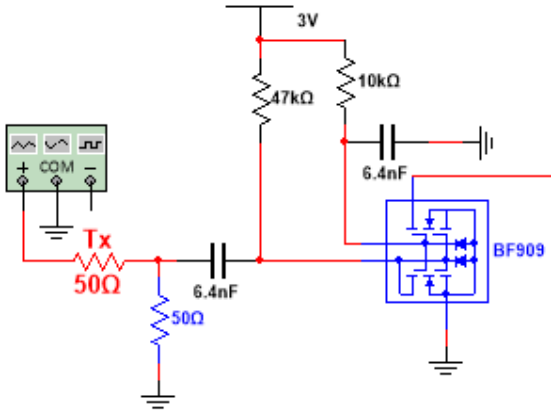



**Fig. 4 Switch's input configuration**

### *3.1. Parallel Resonance Circuit*

The estimated maximum drain current was 22.5 mA based on the datasheet. The signal from this current might result in being smaller; in this case, a resonant circuit is added to amplify the oscillation current that goes to the MOSFET. Given the values R = 10 kΩ, L = 350 nH, C = 0.03 pF, the resonance frequency can be calculated as [42, 43]:

$$f_r = \frac{1}{2\pi\sqrt{LC}} = 51\ MHz \quad (3)$$

The inductive reactance at the resonance frequency is given as:

$$X_L = 2\pi fL \quad (4)$$

$$X_L = 2\pi(0.87x10^{6})(1x10^{-6}) = 5.47\ \Omega$$

The quality factor:

$$Q = \frac{R}{X_L} \quad (5)$$

$$Q = \frac{10x10^{3}}{5.47} = 1828$$

To calculate the range of frequencies from the peak resonance frequency, the calculation of the bandwidth is required as:

$$BW = \frac{f_r}{Q} \quad (6)$$

$$BW = \frac{0.87x10^{9}}{1828} = 1\ MHz$$

The lower peak frequency is the distance from the resonance frequency by bandwidth.

$$f_L = f_r - BW \tag{7}$$

$$f_L = 51\text{MHz} - 1\text{x}10^6 = 50\ MHz$$

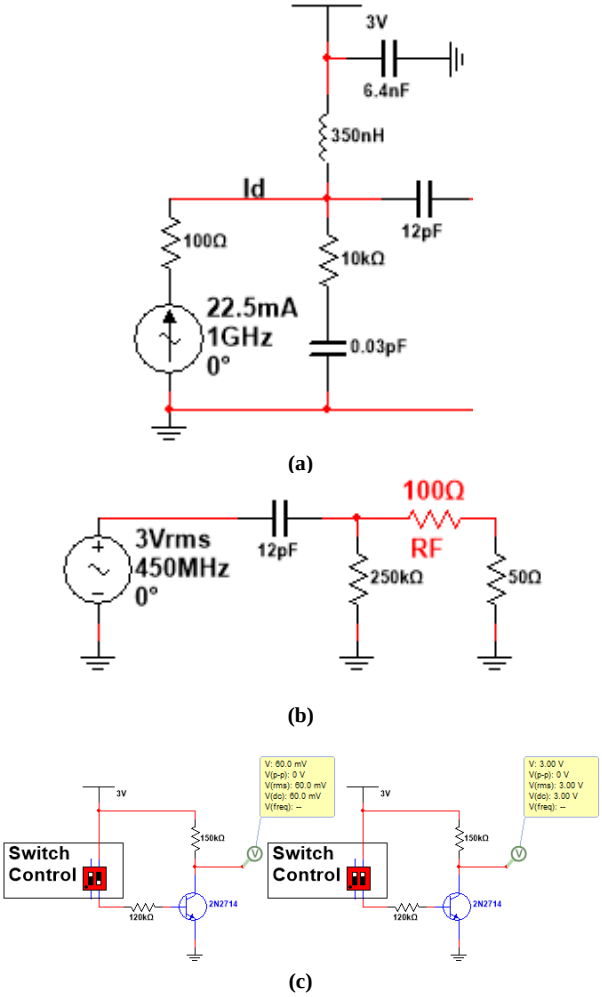



**Fig. 5 (a) Resonant circuit, (b) High pass filter at the output, and (c) NOT gate implementation**

Figure 5 shows the resonance circuit, which can amplify voltage output by rejecting the current of frequencies close to the resonance frequencies. The circuit has a 6.4 nF coupling capacitor to reject any DC voltage passing through the 3 V supply.

### *3.2. Output High Pass Filter*

The receiver and the transmitter share the RF port of the system. When the double-gate MOSFET of the transmit side is OFF, a very small voltage change is seen at the RF port. This might affect isolation; therefore, the system has to ensure that the signal changes from the transmit do not interfere with signal input at RF when the system is turned into receiver mode. A high pass filter is inserted at the output of the transmit side so that a low-frequency signal is filtered. The high pass filter is most significant at the transmitter output, although this is inserted at the output of the receiver side. This reason is for both the transmitter side and the receiver side. Since the system works with high-frequency signals, any cause that might cause DC or lower frequency distortion must be eliminated. A high-pass filter is inserted on both sides to reduce the effects of lower-frequency signals.

For the system, the same parameters or elements of the transmit side are applied to the receiver side. To calculate the cut-off frequency of the high pass filter used at both ends:

$$f_c = \frac{1}{2\pi RC} \tag{8}$$

$$f_c = \frac{1}{2\pi(250\text{x}10^3)(12\text{x}10^{-9})} = 53\ kHz$$

### *3.3. Switch Control*

A NOT-gate has been implemented to control the gate voltages to reduce the number of control inputs, as shown in Fig. 5(c). When the input control is high, the system is configured as a transmitter, and when there is no input voltage or when the voltage at the control is set to ground, the system (for which it is by default) is set to receiver mode.

For the circuit implementation of the NOT gate, 150 KΩ is used at collector voltage, and 120 KΩ is used at base voltage. From the simulation of the NOT gate, when there is a high voltage at the base of BJT, the output is 60 mV. As missioned earlier, the BF909 gate-2 turns OFF when the voltage is less than 0.5 V, and 60 mV is insignificant enough to turn-OFF gate-2 current. When the voltage at the base of BJT is low, the BJT turns OFF, and 3 V is the output of the NOT gate.

## 4. Analysis of Designed Switch

Figure 6 shows the overall integrated circuit, representing a DP4T switch with DG MOSFET. Differential voltage gain is voltage gain that appears due to a difference in voltage between two input terminals. For the switch to be considered accurate, the voltage loss between transmit input signal ($T_X$) and transmit output signal (RF) must be as minimum as possible for this case. The same goes for receiving an input signal (RF) and receiving a signal output ($R_X$). Loss of input voltage at the output will cause signal distortion. An effective switch would rather have an amplified output signal.

### *4.1. Common mode gain (RF – to – RX)*

At 100 MHz, Output gain = $20\log\left(\frac{2.74}{2}\right) = 2.73$ dB

Figure 8 shows the simulation results for the Rx side of the device. The output of the signal is 2.74 $V_{p\text{-}p}$, and compared to the input signal amplitude of 2 $V_{p\text{-}p}$, the simulation has positive results since there is no signal lost at the output.

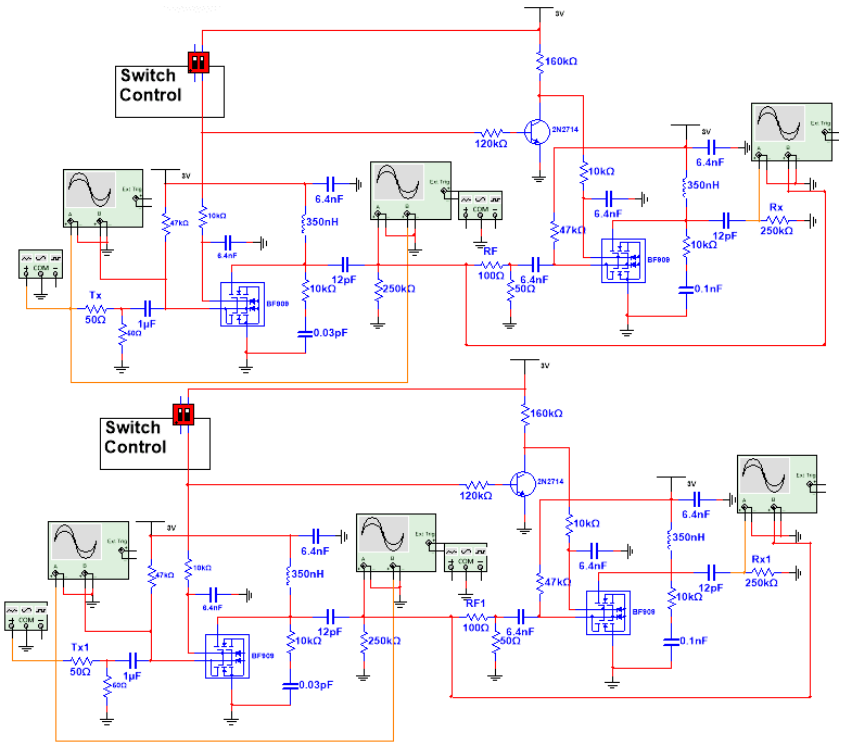
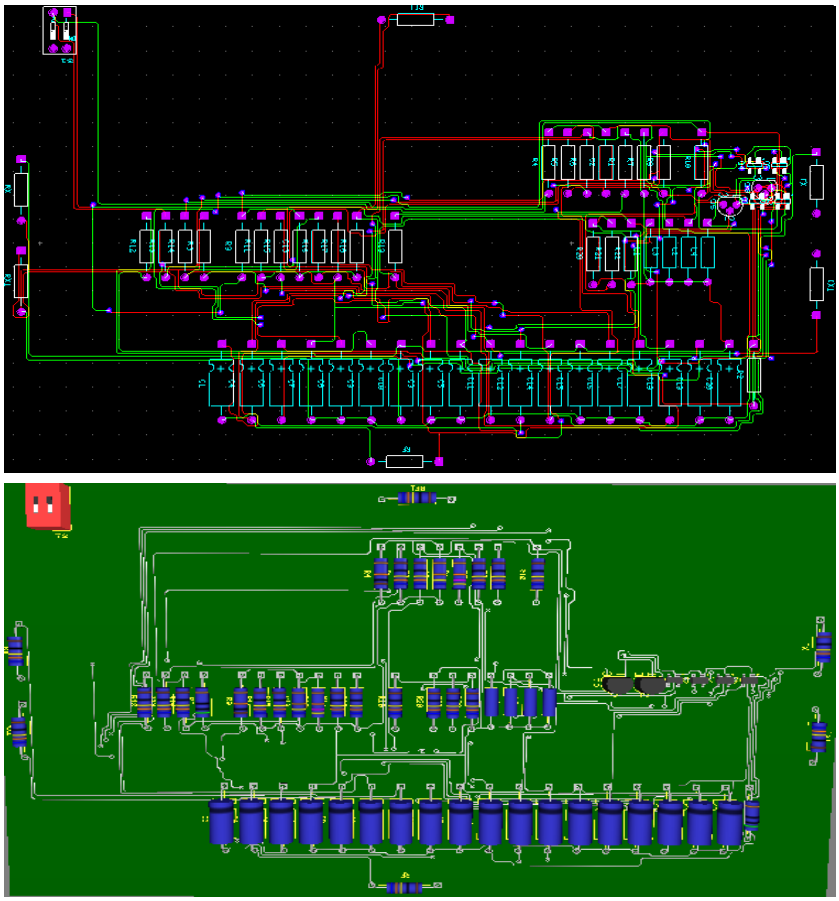


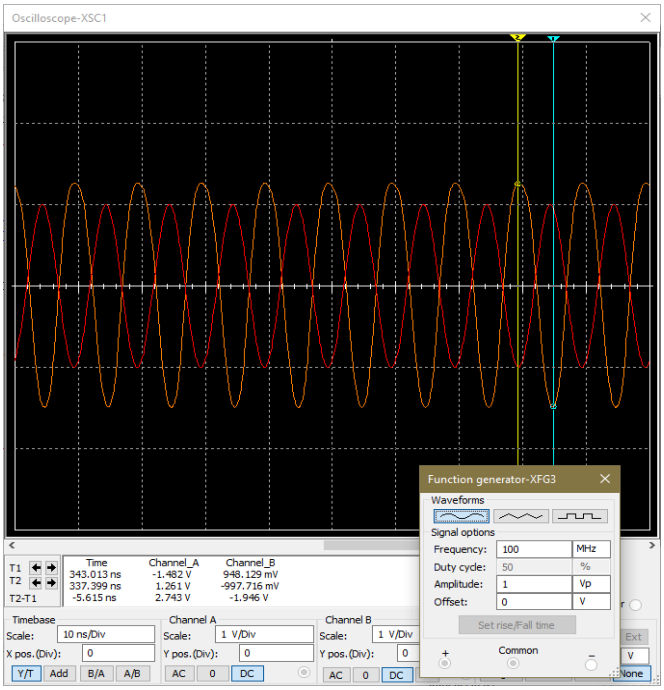

**Fig. 6 Designed DP4T switch (full circuit)**



**(a)**

**(b)**

**Fig. 7 PCB layout (a) design (double layered), and (b) 3D overview**

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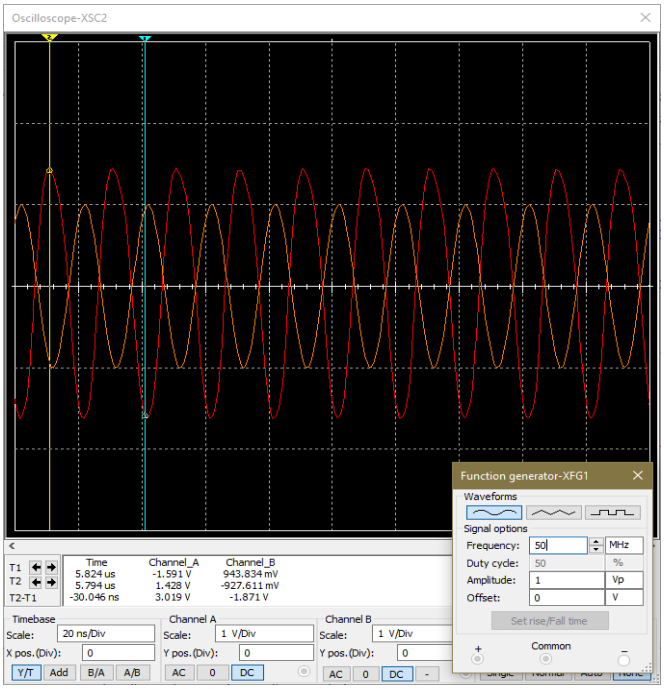
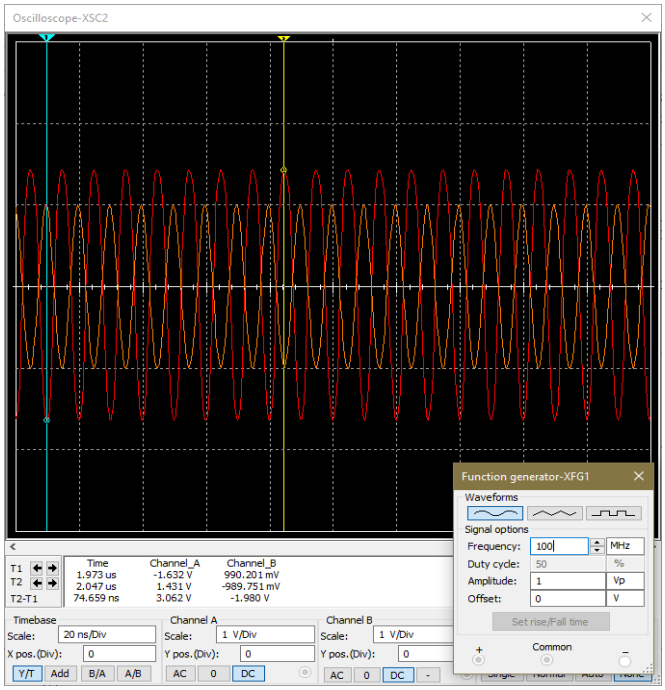



**(b)**

**Fig. 8 (a) Output at 100MHz, and (b) Output at 50MHz.**

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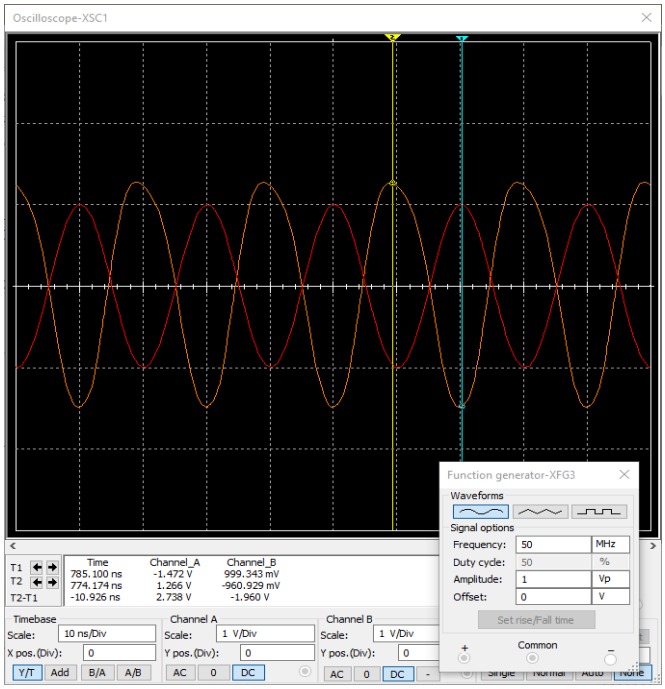



**(b)**

**Figure 9. (a) Output at 50 MHz, and (b) Output at 100 MHz.**

At 50 MHz, Output gain $= 20\log\left(\frac{2.738}{2}\right) = 2.72$ dB

The signal's gain at 50MHz is positive, meaning there is no signal lost at the output.

### *4.2. Differential mode gain TX – RF side*

At 50 MHz, Output $= 20\log\left(\frac{3.019}{2}\right) = 3.58$ dB

At 100 MHz, Output $= 20\log\left(\frac{3.062}{2}\right) = 3.70$ dB

The output signal has a positive gain w.r.t. the input signal, which means no signal is lost during switching. The sine wave at the output is not distorted, so there is no change in the signal period, and the frequencies of output signals are still inserted at the input.

### *4.3. Isolation of the Switch*

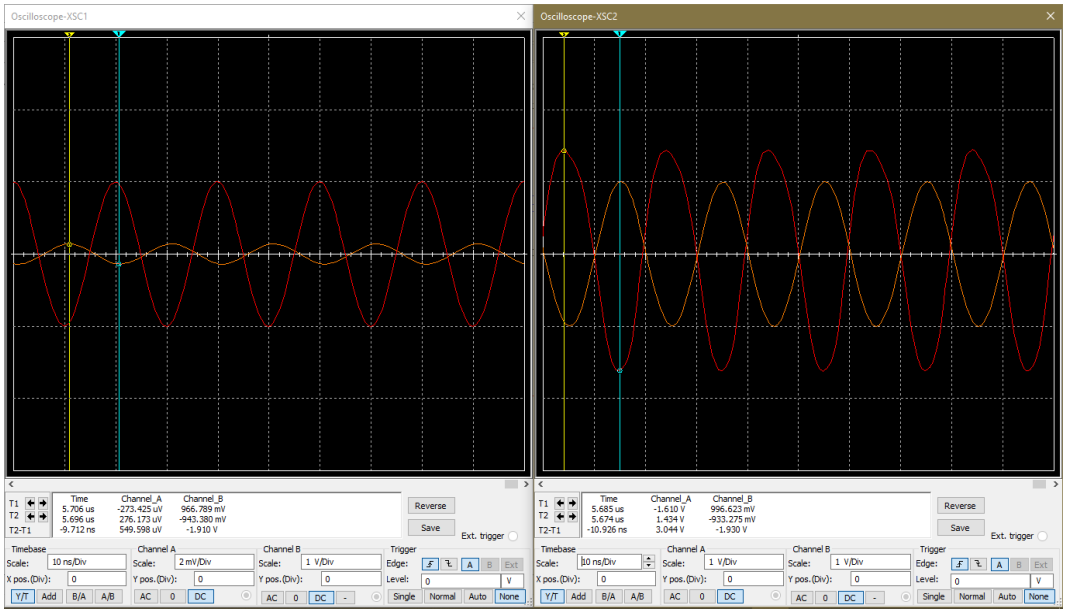
The DP4T switch uses two sections of the SPDT switch circuit, permanently isolated. The only part that needs to be controlled is the interface between the Rx and Tx side of the device, and this can only be controlled by switching the DG MOSFET.

The output of the Tx side and the input of the Rx side share a common terminal, so it is easy for the signal from the Tx side to sip through to the Rx side if not switched effectively. The test was made by disconnecting the interface and testing each side individually. Figure 10 on the left shows the output of the Tx side and the Rx side on the right at 50 MHz and 100 MHz, respectively.

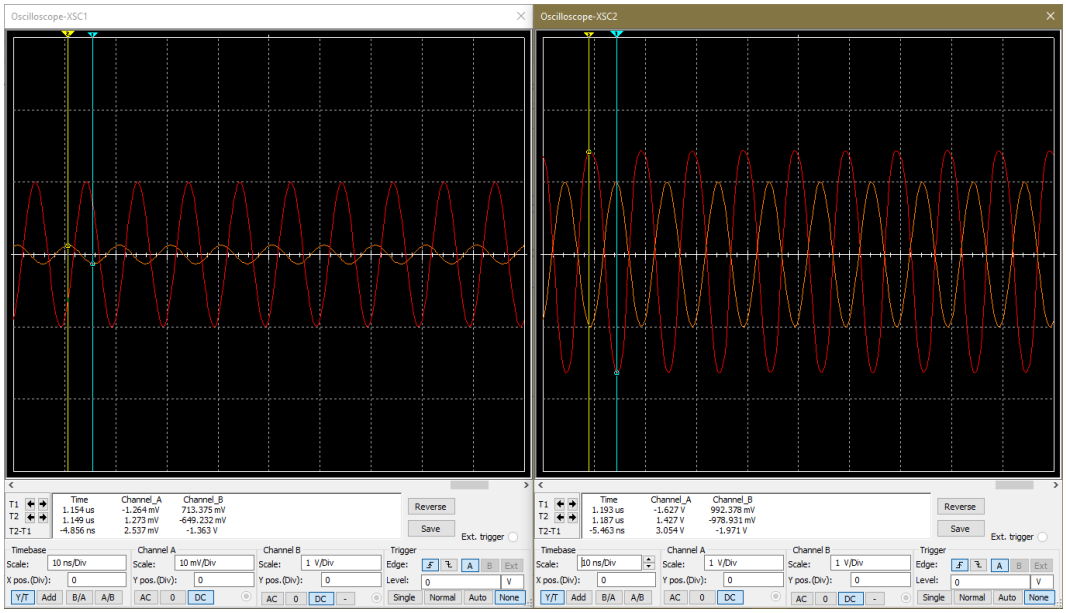
At 50 MHz, Isolation ~70 dB

$$\text{At 100 MHz, Isolation} = 20\log\left(\frac{1}{\frac{2.537\text{m}}{2.437}}\right) = 60\ \text{dB}$$

The largest output peak voltage from the Rx side is 2 mV, which is 2 percent of the input signal of 1 $V_{peak}$. This is relatively insignificant and does not affect the results as missioned earlier that the output signal is a smooth sine wave, and nothing has affected the output signal period.




**(a)**




**(b)**

**Figure 10. (a) Isolation at 50 MHz, and (b) Isolation at 100 MHz.**

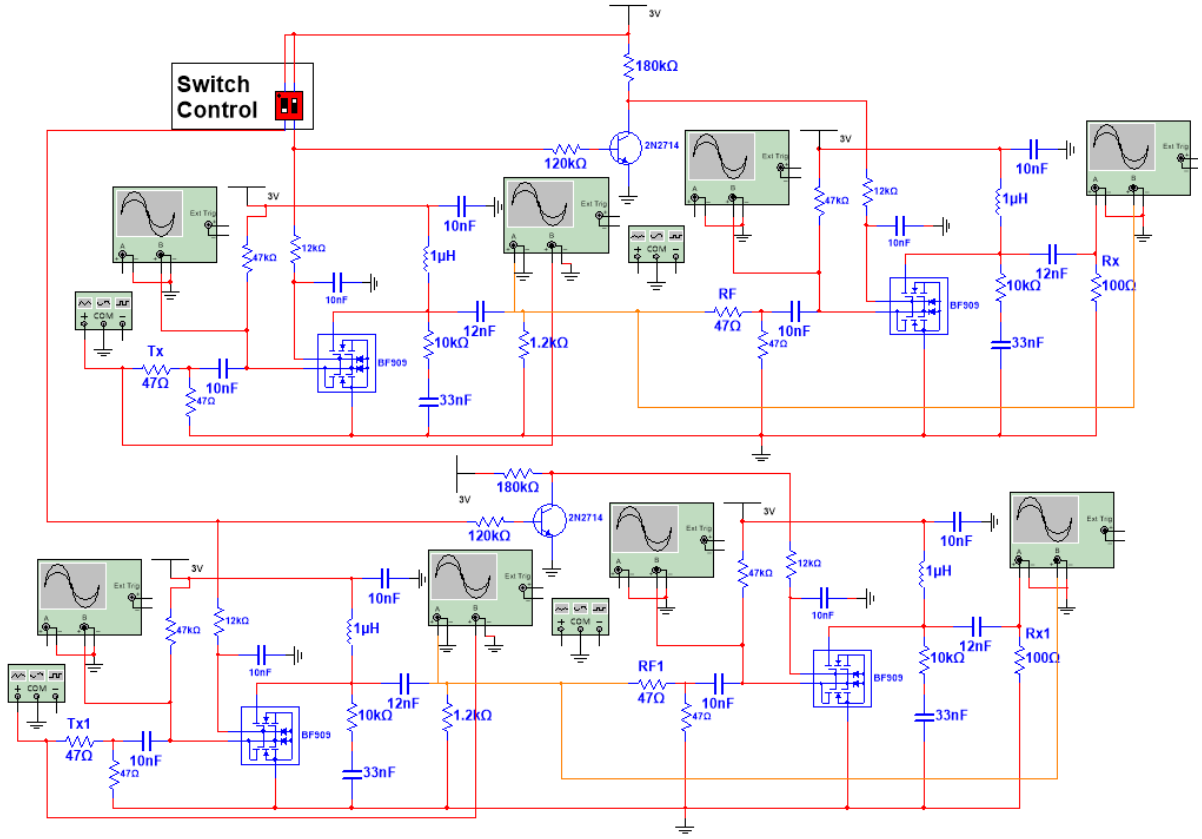
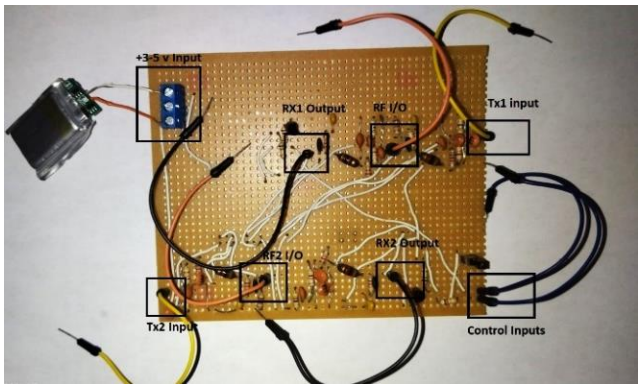



**Fig. 11 Hardware implementation step with standard components.**

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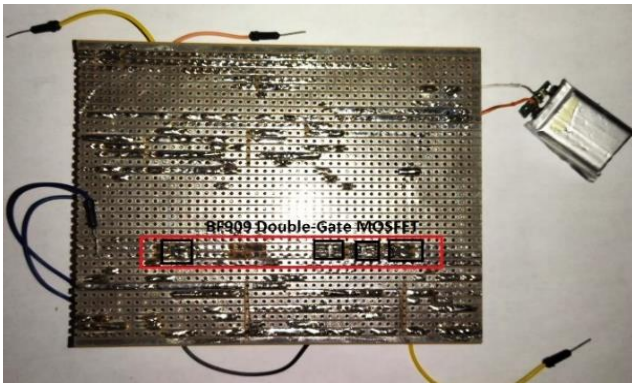



**(b)**

**Fig. 12 Circuit (a) top-view, and (b) bottom-view**

## 5. Prototype Design and Its Validation

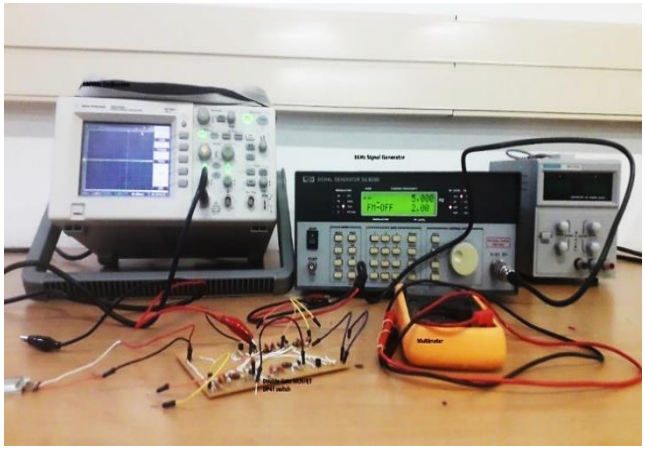
For DG MOSFET with proper gate-1 biasing, the signal could be inserted effectively through gate-1. When the signal is needed, the voltage to gate-2 can be increased to that specific double-gate MOSFET threshold. This is the best topology as it does not need extra components since the signal can be controlled with the gate-2 already embedded in the chip [44-46]. Figure 11 shows the full circuit with standard component values.

The circuit is built with Carbon film resistors, ceramic capacitors, axial inductors/colour ring inductors, etc. The 2N3904 BJT was chosen for the implementation of the NOT gate. The DG MOSFET chip is a surface-mounted BF909, which is 3 mm x 1.4 mm in dimensions, as shown in Figure 2. The prototype has been built on a Vero board. The simulation's 50 Ω or 47 Ω resistor represents the input and output connectors. A *4 V* battery is used as a power supply to the circuit. Figure 12(a) shows the top view of the Veroboard, where all the ports of the circuit have been labeled. The four DG MOSFETs have been connected at the bottom of the circuit since it would be surface mounted to the Veroboard. Figure 12(b) shows the bottom view of the circuit. The workstation for testing the switch requires four main devices 1 GHz Function generator, 100 MHz oscilloscopes, a 5 V power supply, and a multimeter.

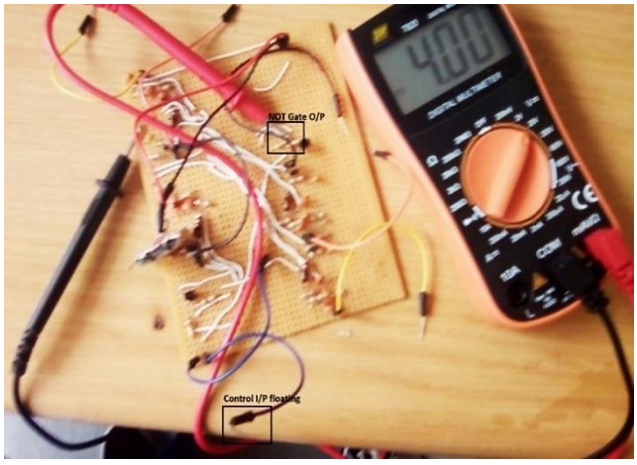
The tested parameters are NOT gate functionality, bandwidth (where or not the switch functions properly between 50 MHz to 100 MHz), and the insertion loss (which is how much of the input signal can be retained at the output).

### *5.1. NOT-Gate Functioning*

When the base (control input) voltage is high, the output of the NOT gate is supposed to be low, and when the control voltage is floating or low, the output of the NOT gate is supposed to be high. Figure 13 shows the results from NOT gate testing, and it shows that when the control input is connected to high voltage, the NOT-gate output is almost zero volts. When the control input is floating, the output is *4 V*. This means the NOT-gate functions properly.



**(a)**




**(b)**

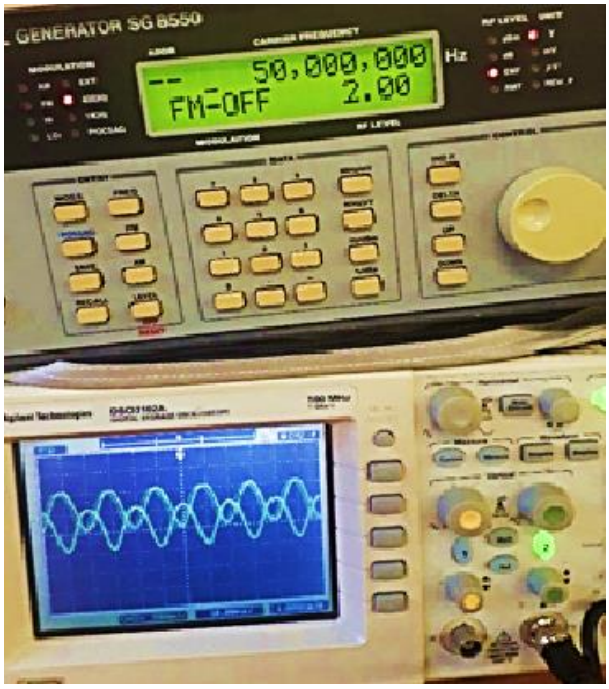
**Fig. 13(a) Workstation, (b) NOT-gate output for control input at 4V.**

### *5.2. Bandwidth and Insertion loss*

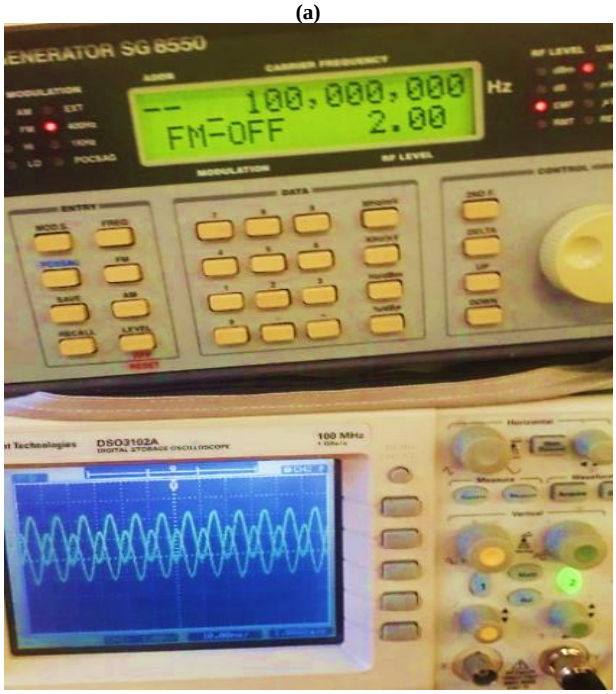
The minimum signal properties required for the switch to function: Signal amplitude *1 V to 3 V* peak signal frequency: 50 MHz < f < 100 MHz. The testing equipment only shows the output signal. Figure 14(a) shows the signal's output from the Tx1 side of the switch. When the input signal is at 50 MHz, the output of the switch is about 1 $V_{peak,}$ and when the input frequency of the switch is at 100 MHz, the output of the switch is at 1.2 $V_{peak}$. Figure 14(b) shows the results obtained from the Rx1 side of the switch. The results are almost identical to those for the Tx1 side of the switch.

$$\text{At 50 MHz, Output} = 20\log\left(\frac{2}{2}\right) = 0 \text{ dB}$$

$$\text{At 100 MHz, Output} = 20\log\left(\frac{2*1.2}{2}\right) = 1.58 \text{ dB}$$




**(a)**




**(b)**

**Fig. 14 Switch outputs at 50 MHz and 100 MHz.**

The signal output at both frequencies is a smooth sine wave, which means there are no interferences with the period of the signal. The output of the signal is at least greater than 1 $V_{peak}$, which means the insertion loss is less than 0% at both frequencies. Since the device works reasonably at the limits of the bandwidth, the device is assumed to give similar results for frequencies between 50 MHz and 100 MHz.

## 6. Conclusion and Future Recommendations

With the rapid growth in communication systems, MIMO systems play a critical role in communication systems infrastructure. As users increase, the technologies must keep up with development, improvement, and traffic management. Most communication systems use RF signals for information transmission; thus, the main criteria are communication infrastructure to handle high-frequency operations. The advancement of technology these days also favors the reduction in the relative size of the device to improve portability while maintaining peak performance and low power consumption. The designed DP4T switch using DG MOSFET proves to be an effective solution since it operates at low power inputs, can handle high-frequency operation, and shows low insertion losses and isolation; these operational aspects produce a high-performance switch that can be integrated with some of the immerging 5G technology. The DP4T prototype switch was designed. Testing results have shown that the switch does not lose any signal at the output, and the output gain was 85% accurate compared to the simulations.

In future, this DG MOSFET can be used with high-dielectric materials such as $HfO_2$. In addition, its application can be discussed.

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