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Original Article

Effects of Voltage Gain and Power losses in Z source Converter Circuit using Zero Voltage Switch

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Abstract *- This research investigates the effect of a zero voltage switch circuit on the capacitance and inductance adjustment in a zero voltage switch circuit for observed peak voltage, peak current, ripple voltage, ripple current and voltage gain in the Z source. The experiment has found that when the capacitance and inductance have changed, which affects peak voltage, peak current, ripple voltage, ripple current and voltage gain.*

Keywords *- Z source circuit, Zero voltage switch circuit, Voltage gain, Ripple voltage, Ripple current.*

1. Introduction

The inverter circuit with a transformer has the advantage of galvanic isolation of the input power supply system from the load or distribution system, as well as the ability to raise the AC voltage obtained after modulating the voltage from the cell. The sun can be easily raised with a transformer. However, because of their size and weight, transformer inverter circuits create shipping and installation challenges. It may be possible to solve this issue by using high-frequency transformers that are smaller and lighter in weight [1-2]. The frequency transformers have a complex power conversion process. Changing the DC voltage to an AC voltage at high frequencies is necessary. The high-frequency AC power must then be transformed down to the regular low-frequency (50–60 kHz) [3], making it a multi-step conversion process that is difficult to produce, costly, and intricate [4].

On the contrary, transformerless inverter circuits have no transformer components. It makes this type of inverter smaller and lighter. In addition, the power conversion process has fewer steps. As a result, this type of inverter has an extremely high power conversion efficiency (greater than 90%) [5]. This transformerless inverter comes in different styles, but it can be broken down into three types based on how the basic circuit works, as follows: voltage source inverters (VSI), current source inverters (CSI), and impedance source inverters (Z source: ZSI).

The Z-source DC-DC boost converter [6–12] is one of the many applications of impedance source circuits. This circuit was first introduced by Xupeng Fang and Xingquan Ji [20] in 2008. The circuit uses a more than three-fold increase in the voltage produced by solar cells. Instead of the power diodes, conductors (S1) are implemented to improve their resistance to reverse voltage. However, the characteristics of the impedance source circuit which relies on the interaction between the two circuits, namely the closing circuit (conducting current) of the switch S2 and the impedance circuit (LC impedance circuit); that is, when switch S2 is off, the supply and load systems are separated (shoot-through state). The supply system feeds power to the impedance circuit, causing the voltage level inside the impedance circuit to grow at a rate determined by the inductor and capacitor values. In the S2 short circuit (conducting stop), the supply voltage plus the voltage drop across the circuit impedance will result in a greater apparent output voltage. It relies on the switch S2's duty cycle (D). The advantages of voltage and current source circuits have gained widespread attention and study in recent years due to the power losses that occur within circuits and devices in on-off conditions. Switching losses for impedance supply circuits tend to be much higher than those without LC impedance circuits. If the design values of inductors and capacitors in the circuit are inappropriate, they are too small. The rate of pressure rising is also higher. To ensure that switching losses are kept to a minimum, the design must be very careful [14–15].

A Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) circuit [16–19] is a circuit that is popularly used to reduce power loss. At the same time, switches are turned on and off through devices such as capacitors, inductors, resistors, or some semiconductor devices.

Together with the switch, they make the unit voltage or current zero while turning on or off the switch [14]. These circuits may also be used to mitigate the effects of voltage spikes on impedance supply circuits. The effects of using these circuits to reduce power loss in impedance supply circuits have not been studied or described in detail. However, since these devices consist of capacitors, inductors, or resistors, they directly affect the change in total capacitance, total inductance, or impedance. That shows up in the impedance circuit and affects the voltage gain of the power converter circuit as a whole. In the study results in this section, no studies have been done, or the effects are detailed. It is the origin of this research study. It will look at how the zero voltage switch (ZVS) circuit changes when capacitance and inductance values are changed. The goal is to develop a DC voltage compounding circuit with an impedance source.

2. Principle and design

This research employs such principles and knowledge to carry out research to achieve specific goals such as proposed circuit structure, working principle, calculating values, and device properties in a circuit. The details are as follows:

2.1. Utilizing a Z-source Converter Circuit Using a Zero Voltage Switch

The proposed Z-source Converter Circuit using a Zero Voltage Switch is shown in Fig. 1. The circuit consists of an impedance source circuit having two inductors and two capacitors. The zero voltage switch consists of two switches and a capacitor astride the switch. The input voltage is 100 VDC. The load resistor is chosen as R1 = 5Ω. The operating principle of the circuit begins with the closure of switch S2 and the impedance circuit (LC impedance circuit); when switch S2 is closed, the supply and load systems are separated (Shoot-through state). The impedance circuit receives energy from the supply system, causing the voltage level to increase at a rate determined by the values of the inductors and capacitors in the circuit. When switch S2 is in the open position, the positive supply voltage and the voltage across the impedance circuit will cause the output voltage of the circuit to increase. When switch S2 is in the open position, the positive supply voltage and the voltage across the impedance circuit will cause the circuit's output voltage to increase by the output voltage depending on the switch S2's duty cycle.

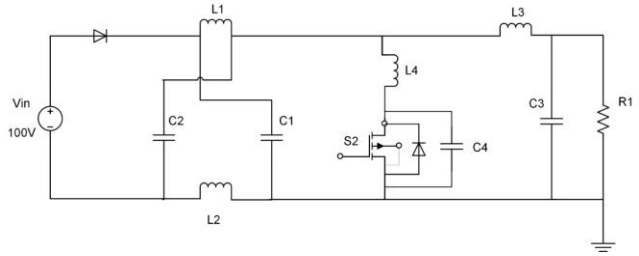

Fig. 1 The proposed circuit

2.2. Calculation and properties of devices in the circuit

The impedance circuit consists of two inductors (L1 and L2) and two capacitors (C1 and C2). The impedance circuit design should be designed at the lowest voltage so that the boost factor B is the highest when there is no boost (non-shoot through). The capacitor voltage of the impedance circuit is equal to the input voltage of the converter, whereas the voltage at the inductor is zero when boosted (shoot through). The current flowing through the inductor is higher, and the voltage at the inductor is equal to the voltage across the capacitor until the boost ends. At the end of the boost, the inductor's current diminishes. The inductor voltage is not equivalent to the capacitor voltage. The average current (I_{L_avg}) at the inductor can be calculated from Equation 1.

$$I_{L\_avg} = \frac{P_{inc}}{V_{PV}} \tag{1}$$

when P_{inc} is the power converter

V_{PV} is input voltage

The design requires that the ripple current flowing through the inductor be 60%. You can find the maximum current, minimum current, and ripple current based on equations 2, 3, and 4.

$$I_{L,\max} = I_L + I_L \bullet 30\% \tag{2}$$

$$I_{L,\min} = I_L - I_L \bullet 30\% \tag{3}$$

$$\Delta I = I_{L,\max} - I_{L,\min} \tag{4}$$

when

$I_{L,max}$ is the maximum current flowing through the inductor.

$I_{L,min}$ is the minimum current flowing through the inductor.

ΔI_L is ripple current

When there is a short circuit, the capacitor voltage is as follows:

$$U_C = \frac{V_{\max} + V_{\min}}{2} \tag{5}$$

when

V_{max} is the maximum input voltage of the converter

V_{min} is the minimum input voltage of the converter

The value of the inductor, as shown in equation 6, can be written as follows:

$$L = \frac{T_{sh} + U_C}{\Delta I_L} \tag{6}$$

The proposed impedance circuit uses inductors with values of L1 = L2 = 160 uH and L3 = 20 uH. The calculated values can be used to make an inductor with a pressed iron powder toroidal core, which has the highest inductance per usable area and the best area-to-volume ratio for heat dissipation. The advantages of the thermocouple core are that it has a self-sealing magnetic field, which makes it less susceptible to interference from other magnetic fields and has a low leakage flux effect.

In impedance circuits, capacitors (C1, C2) are used to smooth out the current and keep the pressure level steady during the shoot-through. In impedance circuits, capacitors reduce current ripple and maintain a steady pressure level. During the shoot-through, the capacitor charges the inductor, and the current through the capacitor is equal to the current through the inductor. The value of the capacitor can be computed as follows, according to equation 7:

$$C = \frac{I_{L,avg} x T_{sh}}{U_C} \tag{7}$$

From Equation 7, the value of the capacitor is quite low. In this study, the circuit uses a capacitor with a value of C1=C2=1000uF/600V, and C3=100uF/600V was used as the film type since these capacitors have the same capacitance as electrolytic capacitors but are smaller and have a higher ripple reduction efficiency.

The power MOSFET with the number IRF3205 was chosen because it has very low resistance between its drain and source ($R_{DS(on)}$ = 0.008). The drain and source pin (VDS) voltage withstands 55 volts. The maximum drain current that can flow through it is 110 amps. The pulse width modulation control circuit operates at a frequency of 20 kilohertz, a frequency that is suitable for use. The signal's duty cycle can be adjusted from 0 to 100%. The power MOSFET gate drive uses the IC TPL250. The frequency pulse width modulation generator circuit sends a signal with a voltage between 0 and 5 volts to the input signal of the circuit by connecting via a 1 kΩ resistance so that the current passing through the light-emitting diode is not so high as to cause damage. The output of the circuit is set to a voltage of 15 volts by receiving voltage from the power supply.

The power loss of the switch while conducting current (P_{cond}) using the approximation can be written as follows:

$$P_{cond} = V_{CEO} x I_{ave} + {I_{ave}}^2 r_d \tag{8}$$

The loss of power incurred while switching on and off an impedance supply circuit with a zero voltage switch, as calculated by Equations (9) and (10).

$$P_{SW-On} = \frac{1}{2T_{sim}} \sum_{t=0}^{T_{sim}} [(V_{CE-on} \cdot I_{C-on}) \cdot t_{on+rr}] \tag{9}$$

when $t_{On+rec} = \frac{2 \cdot (E_{on} + E_{rec})}{(V_{CE} \cdot I_C)}$

$$P_{SW-off} = \frac{1}{2T_{sim}} \sum_{t=0}^{T_{sim}} [(V_{CE-off} \cdot I_{C-off}) \cdot t_{off}] \tag{10}$$

when $t_{off} = \frac{2 \cdot (E_{off})}{(V_{CE} \cdot I_C)}$

3. Results

The z-source converter circuit simulation results use a zero-voltage switch to test how inductors (L_4) and capacitors (C_4) are connected in parallel and series with switches can reduce power losses in impedance supply circuits. The inductor (L_4) is used between 6 uH and 14 uH, and the capacitor (C_4) is used between 6 uF and 14 uF. The proposed circuit uses a duty cycle of 0.3 as the optimal value of the impedance supply circuit. The peak voltage (V_{peak}) after changing the capacitor's values and inductance values. As the value of the capacitor increases, so does the peak voltage (V_{peak}). However, as the inductance adjustment increases, the peak voltage (V_{peak}) tends to decrease, as shown in Table 1.

Table 1. Shows the peak voltage (V_{peak}) values after adjusting the capacitor (C4) and inductance values (L4)

The peak voltage (V_{peak})					
C(uF)	L(uH)				
	6	8	10	12	14
6	369.2	289.9	258.7	238.3	226.9
8	304.8	262.6	239.8	225	214.9
10	281.4	246.9	227.7	216	221.5
12	266.1	234.8	218.4	222.3	227.5
14	251.6	227.2	221.3	221.5	233.9

The circuit has adjusted the capacitor (C4) value and inductor (L4). It can be seen that the higher the capacitor value, the higher the peak current (Ipeak) value, while the higher the inductance adjustment, the less peak current (Ipeak) tends to drop, as shown in Table 2.

Table 2. Shows the peak current (I_{peak}) values after adjusting the capacitor (C_4) and inductance values (L_4)

The peak current (I_{peak})					
C(uF)	L(uH)				
	6 uH	8 uH	10 uH	12 uH	14 uH
6	152.7	110.7	91.3	80.7	73.8
8	145	116.7	101.9	92.6	85.4
10	153	128.2	114.2	104.7	102.9
12	164.6	140.5	125.7	122.6	118.5
14	176.6	152.9	144.2	138.2	134.2

The circuit in Fig. 2 has adjusted the value of the capacitor and inductance settings to affect the ripple output voltage. The data will be summarized into two periods: the range where the output ripple voltage tends to decrease for capacitor values between 6 uF and 10 uF, and the range where the output ripple voltage tends to increase for capacitor values between 12 uF and 14 uF. As seen in Figure 3, the output ripple voltage value is obscure.

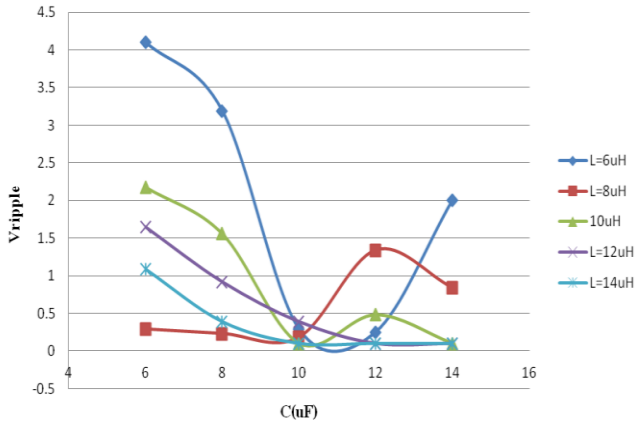

Fig. 3 Shows the ripple voltage values (V_{ripple}) after adjusting the capacitor (C_4) and inductance values (L_4).

Figure 4 shows the ripple current (I_{ripple}) when the capacitor and inductance values are adjusted. The higher the capacitor's capacitance, the lower the ripple current. The ripple current is reduced in the case of adjusting the inductance more.

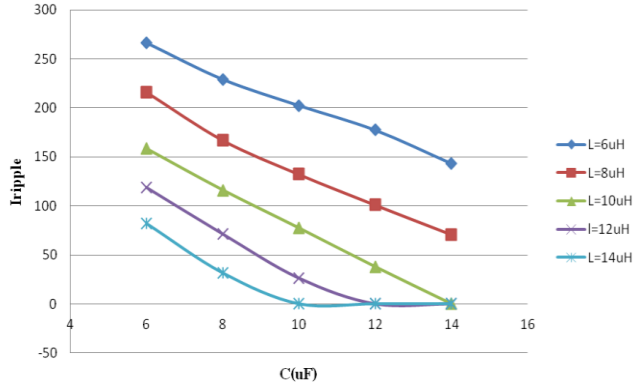

Fig. 4 the ripple current (I_{ripple}) values after adjusting the capacitor (C_4) and inductance values (L4).

Figure 5 shows the voltage gain when the capacitor and inductance values are adjusted. The higher the capacitor's capacitance, the lower the voltage gain. The voltage gain is reduced in the case of adjusting the inductance more. The current-conducting switching losses (P_{cond}) of the z-source converter circuit use a zero voltage switch. The P_{cond} of the z-source converter circuit use a zero voltage switch is 0.7 V. The average current is obtained from the mean of the current flowing through the IGBT simulation of 66.9 A.

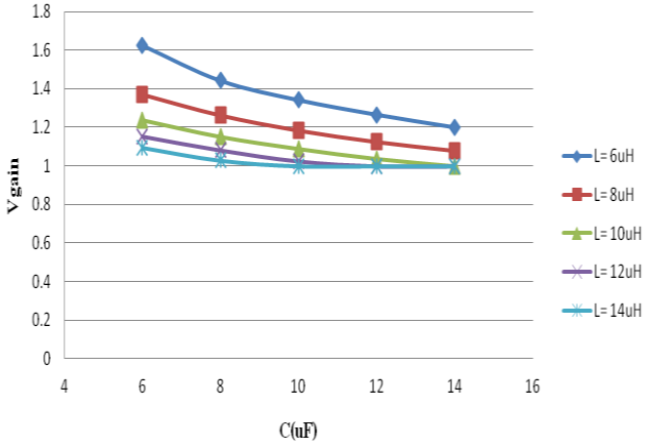

Fig. 5 Shows the voltage gain after adjusting the capacitor (C_4) and inductance values (L_4).

The r_d is $0.031\,\Omega$, and the P_{cond} is 185.57 W. The power loss of the switch during current flowing in the z-source converter circuit uses a zero voltage switch. If the capacitor is constant, but the inductance is increased, it is found that the power loss of the switch during current conduction is increased. But on the other hand, if the inductance is constant and capacitor values are increased, it is found that the power loss of the switch during conduction flow increases, as shown in Figure 6.

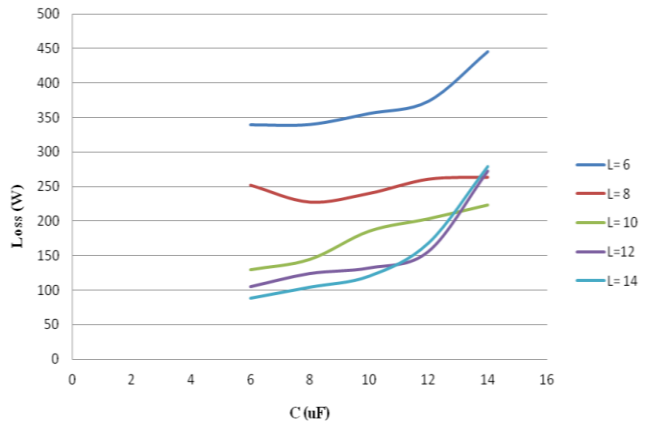

Fig. 6 Shows the current-conducting switching losses (P_{cond}) of the z-source converter circuit

Table 3 shows the power loss when the switch opens the circuit. The power loss value in Table 3 is 0 because its calculated value is -108526.47uW below zero. Table 4

shows the power loss when the switch closes the circuit. Table 4 shows the power loss when the switch closes the circuit. The power loss value is 55084.05 uW when adjusting the inductor between 6 uH and 14 uH. Power loss isn't always the same, which may be because the simulation waveform isn't stable.

Table 3. Shows the power loss when the switch opens the proposed circuit.

ZVS	C(uF)	The power loss when the switch opens				
		6uH	8uH	10uH	12uH	14uH
-108526.47uW	6	0	0	0	0	0
	8	0	0	0	0	0
	10	0	0	0	0	0
	12	0	0	0	0	0
	14	0	0	0	0	0

Table 4. Shows the power loss when the switch closes the circuit.

ZVS	C(uF)	The power is loss when the switch closes the circuit.				
		6uH	8uH	10uH	12uH	14uH
55084.05 uW	**6**	644.94 uW	385.42 uW	172.44 uW	145.58 uW	159.93 uW
	8	252.45 uW	109.31 uW	212.99 uW	134.34 uW	110.17 uW
	10	261.64 uW	33.33 uW	212.45 uW	185.74 uW	132.13 uW
	12	256.10 uW	230.74 uW	203.15 uW	143.55 uW	114.44 uW
	14	156.71 uW	224.29 uW	145.58 uW	209.34 uW	152.63 uW

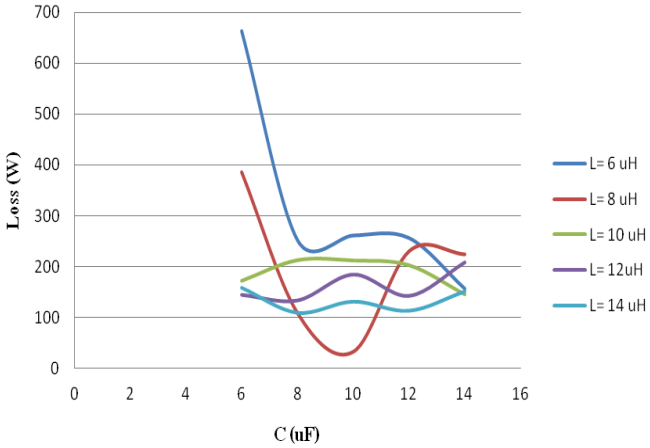

Fig. 7 the power loss when the switch closes the circuit when adjusting the inductor between 6 uH and 14 uH

4. Summary and discussion

The experimental results of the Z-source converter circuit using a zero voltage switch by adjusting capacitance from 6 to 14 uF and inductance from 6 to 14 uH. Peak voltage (Vpeak) reduces from 369.2 V to 233.9 V, and peak current (Ipeak) decreases from 152.7 A to 134.2 A for values of D between 0.1 and 0.4. The output ripple voltage (Vripple) decreases from 4.10 V to 0.1 V. The ripple current at the output (Iripple) decreases from 266.6 A to 0.5 A. The output voltage gain drops from 1.6 to 1. Consequently, the loss of power of the switch during conduction decreased from 339.99 W to 279.03 W. Still, in terms of increasing the inductance, the conduction loss was increased by 445.00 W. Finally, the loss of power when turning the switch on and off was reduced from 644.94 W to 152.63 W. This can reduce the impact of voltage spikes on the impedance supply circuit. Increasing the duty cycle increases the switch's gain and thus its voltage, which may cause switch device damage.

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