International Journal of Engineering Trends and Technology
ISSN: 2231 – 5381 / https://doi.org/10.14445/22315381/IJETT-V70I8P202

Volume 70 Issue 8, 10-25, August 2022

Original Article

Ku Band Ultra-Low Phase Noise PLL Frequency Synthesizer using 0.18 µm CMOS Process

Shobha N. Pawar[1], Pradeep B. Mane[2], Milind P. Gajare[3]

[1]*Department of E&TC Engineering, AISSMS's Institute of Information Technology, Pune, Maharashtra, India.*
[2]*AISSMS's Institute of Information Technology, Pune, Maharashtra, India.*
[3]*Department of E&TC Engineering, AISSMS's Institute of Information Technology, Pune, Maharashtra, India.*

[1]shobha.n.pawar@gmail.com

Received: 24 May 2022 Revised: 26 June 2022 Accepted: 09 July 2022 Published: 09 August 2022

Abstract *- In this era of technology scaling, it is of prime importance to design a frequency synthesizer on a single chip to be used as a frequency multiplying transceiver. Presently, work is unavailable for the entire Ku (12 to 18GHz) band. Single-chip, wideband synthesizers are not available. Whereas in available wideband high-frequency PLL chips, entire elements are not integrated on a single chip, VCO or loop filters are externally connected. This paper presents a 12-18 GHz charge pump-based type-2, integer-N Phase Locked Loop-based frequency synthesizer designed on a single chip using0.18 µm CMOS technology. This PLL is intended to be used as the local oscillator (LO) in potential satellite communication applications. The rigorous phase noise analysis of the PLL in terms of out-of-band and in-band phase noise is performed. This suggests the requirement of block-wise performance improvement for extenuating the practical limits imposed during CMOS layout. Measurement results show that the size of the fabricated chip is only 0.076mm^{2,} which can scale down to 50% by connecting Voltage Controlled Oscillator (VCO) outside the chip. Outstanding phase noise of -122.83dBc/Hz is measured at 1MHz offset when running at14.28GHz oscillation frequency. Process Voltage Temperature (PVT) corner analysis gives a worst-case phase noise of -120.59dBc/Hz and best case phase noise of-124.19dBc/Hz@1MHz offset, which makes implemented chip suitable for satellite communication applications. The dead zone of the Phase Frequency Detector (PFD) is reduced to 1psalong with the negligible charge pump current mismatch ratio of 0.13%. The circuit achieves a fabulous dynamic range of 0.3V to 0.9 V.*

Keywords *- Phase Locked Loops (PLL), Type-2 PLL, Phase Noise, Ku-band, Voltage Controlled Oscillator (VCO).*

1. Introduction

The role of Satellites in global communications is increasing at an unprecedented pace; this transceiver has become the most commonly used circuit. Different frequency bands are used in satellites for uplink and downlink communication to avoid data interference. Carrier frequencies and data rates are continuously increasing with each generation of communication technology. To save the size, power consumption, and cost of the communication system, it is beneficial to use the same synthesizer to generate uplink and downlink frequencies with minimum settling time. To generate a stable, on-chip well-timed RF range of carrier frequencies, phase-locked loops (PLLs) are used as frequency synthesizers in the transceivers [1].

PLL design is challenging because of the mixed-signal nature of the analogue and the digital blocks on the same chip and variations in operating frequency from one block to another [2]. It is highly demanding to design high-frequency mixed-signal circuits on a single chip because of the effect of parasitic elements (resistors and capacitors) and the use of inductors and capacitors in VCO design [22]. PLL must compensate for frequency variations due to changes in PVT corners to generate stable frequency. PVT corners include process variations, supply voltage change, temperature variations, and contribution of low-frequency noise in VCO.

In a charge pump-based integer-N PLL frequency synthesizer output frequency(f_{out}) is an integer multiple of the input reference frequency(f_{ref}),$f_{out} = Nf_{ref.}$Where N is the divide ratio, and the frequency resolution of the PLL is equal to thef_{ref}. As stated by [3], the conventional PLLs with low reference frequency exhibits certain disadvantages as follows: Firstly, the lock time is largely because of its narrow loop bandwidth($f_{BW} = f_{ref}/10$). Secondly, the reference spur, along with its harmonics, are present at low offset frequencies$\left(Referencespur\alpha\Delta I_{CP}\frac{f_{BW}}{f_{ref}}\right)$, where$\Delta I_{CP}$ Is the charge pump mismatch current? Third, PLLs exhibit an increase in in-band phase noise by $20\log(N)\ dB$associated withf_{ref}, the phase frequency detector (PFD), the charge pump (CP), and the divider because of the high divide ratio(N). Low phase noise can be achieved by using high-order filters, but it affects the loop's phase margin; the reverse

approach is to use the smaller loop bandwidth. Still, the downside is it increases the settling time of the PLL, which is not acceptable in satellite communication applications. This states that VCO phase noise will not be adequately suppressed at low offset frequencies with an optimal loop bandwidth. With the increase in demand for precise and faster synthesizers, it becomes difficult for charge pump(CP) PLLs to fulfil these requirements; besides these limitations, it has been noticed that the CP PLLs cannot get replaced with other synthesizers due to their advantages like low design cost, small size, flexibility and stable operation [4,11,12].

As shown in figure1, the Charge Pump PLL is a mixed signal system consisting of various digital and analogue blocks attached in a loop to synchronize generated high-frequency signal with the low reference frequency$\left(f_{ref} = \omega_{ref}/2\pi\right)$. The phase frequency detector (PFD) compares the incoming signal's phase and frequency and generates an error signal (ϕ_e), $\phi_e = K_{PFD}\left[f_{ref} - (f_{out}/N)\right]$PFD's discrete output is translated into a measurable electrical signal using a charge pump (CP) circuit. The output of the charge pump is used to charge and discharge the filter capacitor. As the charge on the capacitor varies, the voltage V_{CL} On it integrates the error signalϕ_e. $V_{CL} = K_{cp}\int \phi_e\, dt$,$K_{cp}$ Is the charge pump gain? To dampen high-frequency harmonics, a low pass filter has been implemented as a loop filter (LF). This loop filter produces a control voltage(V_C) To drive voltage-controlled oscillator (VCO).

$$V_C = K_{cp}\int \phi_e\, dt = \frac{I_{cp}}{2\pi C_L}\int \left(\phi_{ref} - \phi_{out}\right)/N\ .dt \qquad (1)$$

Here $C_L$is the filter capacitor. The VCO generates a sinusoidal signal with a frequency (f_{out})proportional toV_C.Integer-N divider is implemented in a feedback path for frequency synthesis.

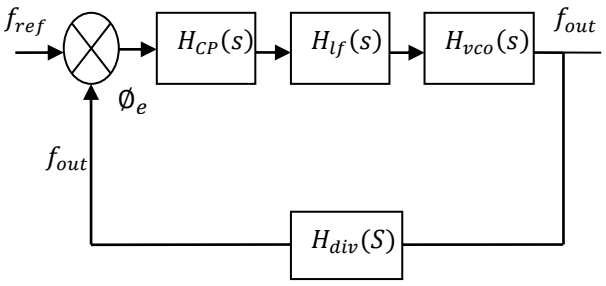

Fig. 1 PLL architecture

E.Ali et al.[32] proposed use of fully digital tri-state PFD generating three states UP, DOWN (DN) and NULL with a wide phase tracking range of $\pm 2\pi$. Sharkia et al.[8] has proposed the use of the gain boosting technique in the forward path for improvement in lock range and tracking of the synchronous peak of the VCO control voltage for reference spur reduction in type-I PLL. Paper suggests using an all-digital voltage-mode topology without a charge pump. The designed PLL chip generates frequencies from 2.2 to 2.8-GHz and achieves in-band phase noise of -103.4 dBc/Hz along with a reference spur of -65dBc.Zhang et al.[9] has proposed a PFD with an improved fast acquisition for high-speed PLL. An improved structure with a dynamic latch is suggested for eliminating PFD non-ideal effects like dead zone and blind zone. The PFD proposed occupies an area of 0.0016mm2 with a power consumption of 1.5mW only using 65nm CMOS technology. Circuit simulation result achieves maximum operation frequency up to 5GHz. The achieved PLL acquisition time is 1us. Nanda et al.[37] has proposed using a variable delay element in the feedback path of PFD to remove the dead zone completely. Lia et al. introduce a PFD with delay time control and a low gain VCO. 130 nm 2P6M CMOS process fabricates a 5.7 to 6.0 GHz PLL.Liu et al.[34] has proposed a distributed bias technique to improve the linearity of the wideband oscillator. The proposed oscillator is implemented using 65-nm CMOS technology and achieves a wide frequency tuning from 61.2 to 100.8, then 122.4 to 136.8, and 198.5 to 273.6 GHz, along with a phase noise of -95.4 dBc/Hz at 1MHz offset. Liao et al.[31] presents a two-stage millimetre wave frequency synthesizer. In the first stage, the implemented circuit performs low phase noise (PN) synthesis; in the second stage, it performs the mm-wave frequency synthesis. Partially depleted silicon on insulator (PDSOI) 45 nm CMOS technology is used for synthesizer prototype fabrication. The 9 GHz RSPLL in the first stage achieves 144 fs integrated jitter and 7.2 mW power consumption. The overall performance shows integrated jitter of 251 fs with a power consumption of 20.6-mW at 35.84 GHz. Wu et al. [32] proposed split-tuned LC-VCO based on an averaging varactor and a servo loop. This makes the charge-pump current (Icp) inversely proportional to the oscillation frequency's square. 3.1 to 3.9GHz PLL is implemented using 0.13 µm CMOS technology.

Key observations from the reviewed literature are no work is available for the entire Ku (12 to 18GHz) band. Single-chip, wideband (6GHz) PLLs are unavailable; in available wideband high-frequency PLL chips, entire PLL elements are not integrated on a single chip, and VCO or loop filter is externally connected because it consumes maximum chip area. It is also found that VCO is power hungry and contributes maximum noise in the PLL [27-30].PVT variations change PLL performance parameters. Performance parameters include phase noise, power dissipation and settling time. To design a single chip, wideband PLL, applying a single methodology is impossible, but a block-wise performance improvement is required. This paper concentrates on the best suitable topology selection for individual blocks, design and analysis of PLL considering phase noise as the primary performance parameter. The presented work overcomes tradeoffs between VCO tuning range, power dissipation and phase noise by the optimal choice of design parameters which includes loop bandwidth

(decides to settle time of PLL), VCO gain (decides VCO output frequency) and filter order (decides phase noise).

Section 2 gives a phase noise analysis of the PLL. PLL architecture is presented in section 3, PLL implementation is given in section 4, Measurement results are shown in section 5, and the paper is concluded in section 6.

2. Phase Noise Analysis of the Pll

PLL phase noise can improve out-band and in-band phase noise performance. The in-band phase noise is the combination of phase noise contribution of PFD, CP, LF and N times the phase noise of the input reference signal. VCO phase noise dominates the out-band phase noise of the PLL[26]. A higher order or lower bandwidth loop filter can minimise out-band phase noise, and a lower division value N can be used to improve in-band phase noise performance. Still, it gives poor frequency resolution, so the trade-off exists between in-band phase noise performance and frequency resolution. Another key challenge in mm-wave frequency synthesizers is; that for the sake of the generation of low noise high-frequency carrier signals, the worsened quality factor of LC tank charge high power consumption along with a narrower frequency locking range. It is important to analyse the contribution of the individual PLL block to implement PLL with ultra-low phase noise. In this paper noise contribution of each block is presented separately; for calculating the contribution of an individual block, the contribution from other blocks is considered zero. The transfer function of the individual blocks is compared with filter characteristics to identify low pass/ high pass characteristics of the noise added by that block. Individual phase noise analysis of the PLL blocks is presented below.

2.1. Reference Input Noise

In frequency synthesizers, a crystal oscillator is preferred to generate a reference signal; input reference is one of the dominant noise sources in PLL. It makes input phase and frequency vary with time. The transfer function for measuring the phase difference between reference and VCO output is written as:

$$H_{ref}(s) = \frac{\emptyset_{out}}{\emptyset_{ref}} = \frac{F(s)\times K_{pfd}\times\frac{K_{vco}}{s}}{1+F(s)\times K_{pfd}\times\frac{K_{vco}}{N\times s}} \qquad (2)$$

$\emptyset_{ref}$ Is the noise that appears at the input of the PFD. If used, this noise is the combination of noise components from crystal oscillator and reference divider.$\emptyset_{out}$ Is the noise which appears at the PLL output [16-17]. Behaviour of the reference signal is checked by comparing equation2 with any filter,$F(s)$. For slow variations in the input phase($s \to 0$), $H_{ref} \to N$. Transfer function settles down to divide ratio N, and for fast variations, it settles down to 0; this indicates PLL does not respond to high reference frequency variations. This concludes that the noise added by input reference has low pass characteristics.H_{ref} Corresponds to division ratio(N) multiplied by low pass filtering of the reference noise.

2.2. PFD Noise

The noise contribution of an error detector (PFD)is negligible compared with the reference signal.PFD transfer function is given by:

$$H_{pfd}(s) = \frac{\emptyset_{out}(s)}{\emptyset_{pfd}(s)} = \frac{F(s)\times\frac{K_{vco}}{s}}{1+F(s)\times K_{pfd}\times\frac{K_{vco}}{N\times s}} \qquad (3)$$

$\emptyset_{pfd}(s)$ Does the PFD add the noise? At low frequencies $s \to 0$transfer function converges to (N/K_{pfd}) which indicates that at low frequencies, PFD noise will get added to PLL output multiplied by $\frac{N}{K_{pfd}}$And the contrary, at high frequencies ($s \to \infty$) transfer function reduces to 0 with $-20dB$slope, indicating that phase detector noise is not a major contributor to PLL output beyond the loop bandwidth.

2.3. CP Noise

Ideally, when PLL is locked, the current transfer to the loop is zero. In reality, CP noise current gets added to the loop filter during non-zero CP current. Current mismatch during UP and DOWN pulses lead to injection of noise current into the loop filter; the noise current can be calculated as:

$$i_{n_{cp}}^2 = 2 \times \frac{\tau}{T_{ref}} \times I_{CP,noise}^2 \qquad (4)$$

$\tau$is the width of UP/DOWN current pulses in lock state.T_{ref}Is the period of input reference.$I_{CP,noise}$Is the current noise density of CP. It is noticed from the equation4that magnitude of the current noise density ($I_{CP,noise}$) is directly proportional to the charge pump's reference input frequency and duty cycle. Hence, switching between UP and DOWN current pulses at high frequencies becomes very critical. The transfer function of CP can be written as:

$$H_{CP}(s) = \frac{\emptyset_{out}(s)}{i_{n_{cp}}(s)} = \frac{2\pi}{I_{CP}} \times \frac{F(s)\times K_{pfd}\times\frac{K_{vco}}{s}}{1+F(s)\times K_{pfd}\times\frac{K_{vco}}{N\times s}} \qquad (5)$$

At low frequencies (within loop bandwidth)($s \to 0$), $H_{CP}(s)$reduces to$20\log\left(\frac{2\pi N}{I_{CP}}\right)$. This indicates the low-frequency noise contribution amplitude is multiplied by$20\log\left(\frac{2\pi N}{I_{CP}}\right)$. Whereas for frequencies beyond loop bandwidth($s \to \infty$)The transfer function settles down to 0 with $-20dB$ slope. It concludes that the CP noise is dominant within loop bandwidth and negligible outside the loop bandwidth. CP non-ideal effects contribute to reference spur; however, they are not critical in CP noise contribution.

2.4. LF Noise

The Loop filter's transfer function is written as:

$$H_{lf}(s) = \frac{\emptyset_{out}(s)}{\vartheta_{lf}(s)} = \frac{\frac{K_{vco}}{s}}{1+F(s)\times K_{pfd}\times\frac{K_{vco}}{N\times s}} \quad (6)$$

$\vartheta_{lf}(s)$ is the loop filter's noise voltage. LF's noise transfer function depends on the order of the low pass filter; for 1st order loops$F(s) = 1$, $H_{lf}(s)$ Becomes:

$$H_{lf}(s) = \frac{\emptyset_{out}(s)}{\vartheta_{lpf}(s)} = \frac{K_{vco}}{s+\frac{K_{pfd}\times K_{vco}}{N}} \quad (7)$$

Filters having a pole and zero; i.e. $F(s) = \frac{1+sT_1}{sT_2}$ Transfer function reduces to bandpass. However, for active filters, the active part also contributes to the phase noise.

2.5. VCO Control Line Noise

The VCO control line power supply noise affects PLL performance; sometimes, supply voltage acts as a control voltage to the VCO. The power supply voltage is the strong source of VCO jitter. The general assumption is supply voltage variation is $\pm 10\,\%$. The dependence of VCO performance on supply voltage is measured as supply gain(K_{VDD}).Phase noise added by supply noise is given by:

$$S_{\emptyset vdd}(s) = \frac{K_{vDD}^2}{f^2} S_{vN_{vdd}(s)} \quad (8)$$

Equation 8 shows the effect of impulsive supply noise on the oscillator's phase noise. The noise transfer function is written as:

$$H_{vDD}(s) = \frac{\emptyset_{out}(s)}{\emptyset_{vDD}(s)} = \frac{\frac{K_{vco}}{s}}{1+F(s)\times K_{pfd}\times\frac{K_{vco}}{N\times s}} \quad (9)$$

It is observed from equation 6 and equation 9 that$H_{vDD}(s)$is similar to$H_{lf}(s)$. It is concluded that it has band pass characteristics, and the low-frequency components will get rejected by the loop.

2.6. VCO Noise

The dominant source of noise in the expected frequency band is a VCO phase noise; the transfer function can be given as:

$$H_{vco}(s) = \frac{\emptyset_{out}(s)}{\emptyset_{vco}(s)} = \frac{1}{1+F(s)\times K_{pfd}\times\frac{K_{vco}}{N\times s}} \quad (10)$$

for 1st order loops as $(s \to 0)$, $H_{vco}(s) = 0$ and $H_{vco}(s) = 1$ when$(s \to \infty)$.For filters having a pole and zero; $F(s) = \frac{1+sT_1}{sT_2}$, It can be stated from equation (10)that for fast changes in the VCO input phase, VCO phase noise contributes to PLL with a gain of 1; the basic solution is to increase the loop bandwidth, which lowers the lock time of the PLL and also gives unstable control voltage for higher frequencies, at the same time to suppress reference spur and to achieve stable loop, loop bandwidth must be smaller than reference input. A strict trade-off is noticed between low phase noise and the spurious level.

2.7. Divider Noise

It is critical to model the noise behaviour of the divider because of the threshold crossings of the divider output signal. It indicates that the total phase noise of the PLL is affected by the divider only during threshold crossing. The divider transfer function can be modelled as:

$$H_{div} = \frac{\emptyset_{out}(s)}{\emptyset_{div}(s)} = \frac{F(s)\times K_{pfd}\times\frac{K_{vco}}{s}}{1+F(s)\times K_{pfd}\times\frac{K_{vco}}{N\times s}} \quad (11)$$

$\emptyset_{div}(s)$ is the divider noise. Equation 11 shows that this transfer function is similar to the reference signal in equation 2. This result is expected because this is the second input of the PFD. When$(s \to 0)$, $H_{div} \to N$and for $(s \to \infty)$, $H_{div} \to 0$. It shows that the noise from the frequency divider has low pass characteristics and can be attenuated by the loop filter.

2.8. Total PLL Output Phase Noise

Total PLL phase noise can be calculated by combining phase noise contributions of the individual PLL blocks.

$$S_{\emptyset_{out}}(f) = S_{\emptyset_{ref}}(f)\left|H_{ref}(j2\pi f)\right|^2 + S_{\emptyset_{pfd}}(f)\left|H_{pfd}(j2\pi f)\right|^2 + S_{i_{ncp}}(f)|H_{CP}(j2\pi f)|^2 + S_{vlpf}(f)\left|H_{lpf}(j2\pi f)\right|^2 + S_{\emptyset_{vdd}}(f)|H_{vdd}(j2\pi f)|^2 + S_{\emptyset_{vco}}(f)|H_{vco}(j2\pi f)|^2 + S_{\emptyset_{div}}(f)|H_{div}(j2\pi f)|^2 \quad (12)$$

It is observed from equation 12 that at low frequencies, the noise contributors within loop bandwidth are the reference signal, the PFD, the CP, LF and divider, whereas outside VCO dominates the loop bandwidth PLL phase noise. Hence it is of prime importance to analyze and minimize VCO noise contribution to minimize the PLL noise. Various noise models are analysed to optimize phase noise in VCO, and the effect of the VCO noise on PLL performance parameters is checked. Based on this noise analysis, VCO noise reduction techniques are applied.

Weigandt et al. presented the relationship between the RMS of cycle jitter (σ_C) And the single side band phase noise at Δf offset frequency. The relationship is given by equation 13.

$$\mathcal{L}(\Delta f) = \frac{{f_0}^3{\sigma_C}^2}{(\Delta f)^2} \quad (13)$$

Herzerl and Razavi presented dependence of phase noise ($\mathcal{L}(\Delta\omega)$) on RMS value of cycle to cycle jitter (σ_{CC}) as given in (14), here ω_0 is the synthesized frequency.

$$\mathcal{L}(\Delta\omega) = \frac{(\omega_0{}^3/4\pi)\sigma_{CC}{}^2}{(\Delta\omega)^2+(\omega_0{}^3/8\pi)^2\sigma_{CC}{}^4} \quad (14)$$

It is observed that (14) reduces to (13) when $|\omega - \omega_0|>>(\omega_0{}^3/8\pi)\sigma_{CC}{}^2$.

Demir et al. derived the relationship between phase noise ($\mathcal{L}(\Delta f)$) and self-referred sitter ($\sigma^2(\Delta t)$) of an oscillator as given in (15) and (16), respectively.

$$\mathcal{L}(\Delta f) = \frac{f_0{}^2 C}{(\Delta f)^2+\pi^2 f_0{}^4 C^2} \quad (15)$$

$$\sigma^2(\Delta t) = \Delta t.C \quad (16)$$

Jitter and spectral spreading in a noisy oscillator are represented by the constant C in (15) and (16). It is observed that the spectral jitter $\sigma(\Delta f)$ is nothing but an absolute jitter $\Delta T_{abs}(\Delta t)$ in a practical sense.

$$\Delta T_{abs}(\Delta t) = \sqrt{\frac{f_0}{2}}\sigma_{CC}\sqrt{\Delta t} \quad (17)$$

After comparing (16) and (17), I obtained an expression for C as:

$$C = \frac{f_0}{2}\sigma_{CC}{}^2 \quad (18)$$

Putting a value of C in (15) verified the equivalence between (15) and (14).

Leeson's empirical equation appropriately describes an oscillator's noise spectrum for single sideband phase noise; hence a universally accepted Leeson's model is adapted for analysing phase noise in dBc/Hz relative to output level per hertz. Leeson's empirical equation gives sources of noise as given by equation (19)

$$\mathcal{L}(\Delta f) = \frac{FKT}{2P_{avg}}\left[1 + \frac{f_c}{\Delta f} + \left(\frac{f_0}{2\Delta f Q_L}\right)^2\left(1 + \frac{f_c}{\Delta f}\right)\right] \quad (19)$$

Where $\mathcal{L}(\Delta f)$ is phase noise in dBc/Hz, F is a noise factor of the active devices, T is the absolute temperature in ^oK, K is the Boltzmann's constant, $P_{avg}$is an average power of the oscillator,f_c is the flicker corner frequency, Δfis carrier offset frequency, $f_0$is output frequency and $Q_L$is the loaded Q.

The phase noise is presented in dBc/Hz; hence (19) can be rewritten as:

$$\mathcal{L}(\Delta f) = 10\log\left\{\frac{FKT}{2P_{avg}}\left[1 + \frac{f_c}{\Delta f} + \left(\frac{f_0}{2\Delta f Q_L}\right)^2\left(1 + \frac{f_c}{\Delta f}\right)\right]\right\} \quad (20)$$

Equation 20 shows main causes of the phase noise are:

$\left(1 + \frac{f_c}{\Delta f}\right)$: Flicker effect

$\left(\frac{f_0}{2\Delta f Q_L}\right)^2$: Oscillator Q

$\frac{f_c}{\Delta f}$: Phase perturbation

Leeson's empirical equation, as given in (19), shows two ways for VCO phase noise reduction either by increasing Q_L or by increasing P_{avg}. It is always convenient to increase Q_L instead of P_{avg} because P_{avg} is directly dependent onV_{peak} and the best way to improve P_{avg} is by increasingV_{peak}.

$$P_{avg} = \frac{V_{peak}{}^2}{R_o} \quad (21)$$

V_{peak} is the maximum voltage across the LC-tank, but the value of $V_{peak}$is limited to VDD in most of the VCO topologies; hence it is convenient to increase the Q factor of the tank elements to achieve phase noise requirements. This Q factor can be increased by decreasing the gate length of the varactors but will decrease the varactor's capacitance ratio, resulting in a lower tuning range. Most parameters in equation 19 are fixed by the technology and not in the scope of designers; power in the load can be manipulated by tuning tank elements, including inductors and capacitors. For minimal noise, large capacitance and small inductance must be used in the LC tank. The reason is the cross-coupled transistors will see an effective resistance's small value, and the high value of the current will be used for the same voltage swing. With the capacitors' increasing size, their size also increases, and parasitic inductance will dominate the tank inductance. Also, the parasitic inductance of interconnects creates a trade-off between Q-factor and oscillation frequency, as the interconnects rarely achieve Q equivalent to tank inductor.

3. Presented PLL Architecture

It is important to initially discuss the concept of phase locking to understand PLL better. Let's assume two signals $x_1(t) = \cos(\omega_1 t + \emptyset_1 t)$and $x_2(t) = \cos(\omega_2 t + \emptyset_2 t)$The instant phases and frequencies can be written as

$$\beta_1(t) = \omega_1 t + \emptyset_1 t \quad (22)$$

$$\beta_2(t) = \omega_2 t + \emptyset_2 t \quad (23)$$

$$\Omega_1(t) = \frac{\delta[\beta_1(t)]}{\delta t} = \omega_1 + \frac{\delta[\emptyset_1(t)]}{\delta t} \quad (24)$$

$$\Omega_2(t) = \frac{\delta[\beta_2(t)]}{\delta t} = \omega_2 + \frac{\delta[\emptyset_2(t)]}{\delta t} \quad (25)$$

When two signals are phase locked, theirdifferences are con stant in time and almost nonexistent. Hence in locked condition

$$\beta_1(t) - \beta_2(t) = \text{constant} \quad (26)$$

$$\frac{\delta[\beta_1(t)-\beta_2(t)]}{\delta t} = \omega_1 - \omega_2 = 0 \quad (27)$$

A constant phase difference between two periodic signals in a feedback loop can be ensured when a loop reaches a steady state. After achieving the lock in a loop, the frequency difference between the two compared signals reduces to zero. PLLs are most commonly divided into type-1 PLLs and type-2 PLLs.

3.1. Type-1 PLL

The phase transfer function analyses a simple PLL by comparing the phase difference between the input $\emptyset_{ref}(s)$and feedback signal$\emptyset_{div}(s)$.An illustration of a type-I PLL with its respective transfer functions is shown in figure 2.

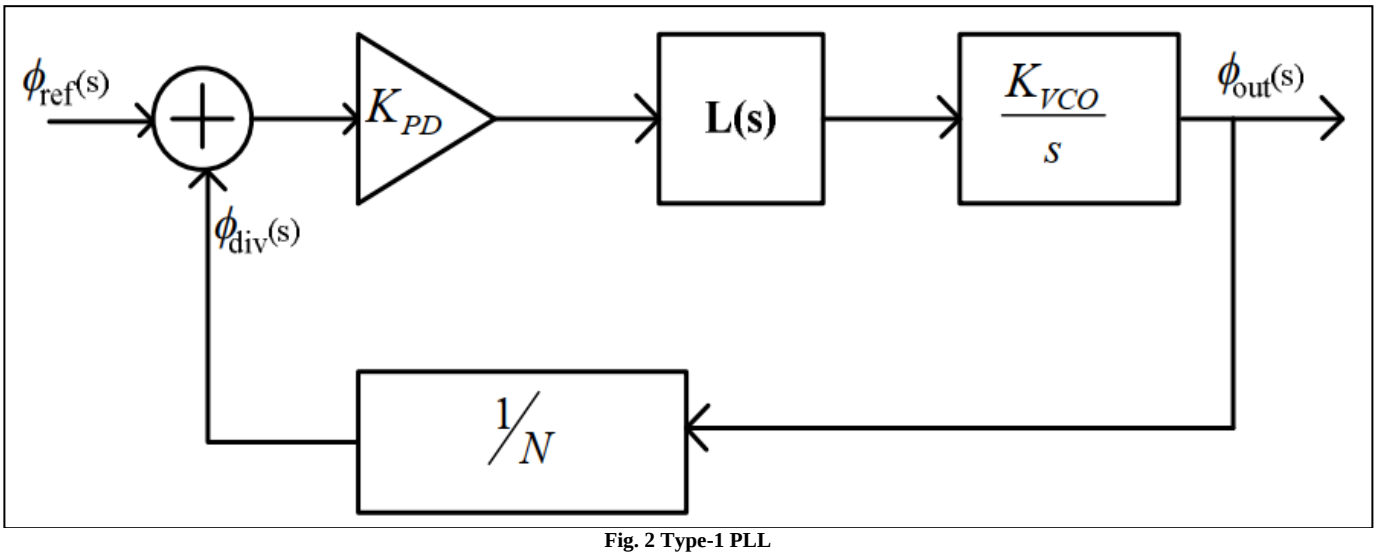

Fig. 2 Type-1 PLL

The transfer function for first order loop filter can be written as,

$$L(s) = \frac{1}{1+s/\omega_{lpf}} \quad (28)$$

Here $\omega_{lpf}$is -3dB bandwidth. The open loop transfer function can be presented as,

$$H_o(s) = \frac{\emptyset_{out}(s)}{\emptyset_{ref}(s)} = \frac{K_{PD}*K_{VCO}}{N} * \left(\frac{1}{s\left(1+\frac{s}{\omega_{lpf}}\right)}\right. \quad (29)$$

As the open loop transfer function contains a single pole at the origin, this type of PLL is called type-I PLL. In case of slow variations in the input phase, giving the pole at the origin, as s reaches zero, loop gain approaches infinity. Hence in locked conditions, PLL confirms that the change in input ($\emptyset_{ref}$) and feedback signal ($\emptyset_{div}$) is the same when s goes to zero. Similarly, the closed-loop transfer is given as,

$$H_c(s) = \frac{\emptyset_{out}(s)}{\emptyset_{ref}(s)} = \frac{\frac{K_{PD}*K_{VCO}}{s^2}}{\omega_{lpf}+s+\frac{K_{PD}K_{VCO}}{N}} \quad (30)$$

This closed-loop transfer function proposes the system can be critically damped, under-damped or over-damped. If we will compare the closed-loop transfer function given by 30 with control theory's standard second order equation given by 31,

$$H(s) = \frac{\omega_n^2}{S^2+2\xi\omega_n S+\omega_n^2} \quad (31)$$

$$\omega_n = \sqrt{\omega_{lpf}K_{PD}K_{VCO}} \quad (32)$$

$$\xi = \frac{1}{2}\sqrt{\frac{\omega_{lpf}}{K_{PD}K_{VCO}}} \quad (33)$$

Here ω_n is the natural frequency and ξ is the damping ratio; the two poles of the closed loop system are presented as $S_{1,2}$.

$$S_{1,2} = \frac{1}{2}\left(\omega_{lpf} \pm \sqrt{{\omega_{lpf}}^2 - \frac{4K_{PD}K_{VCO}}{N}}\right) \quad (34)$$

$$\xi\omega_n = \frac{1}{2}\omega_{lpf} \quad (35)$$

When${\omega_{lpf}}^2 - \frac{4K_{PD}K_{VCO}}{N} > 0$, it means two poles are real transient time response can be given as,$\omega_{out}(t) =$

$$\left[\frac{2K_{PD}K_{VCO}}{\sqrt{{\omega_{lpf}}^2-\frac{4K_{PD}K_{VCO}}{N}}} X \frac{1}{\omega_{lpf}-\sqrt{{\omega_{lpf}}^2-\frac{4K_{PD}K_{VCO}}{N}}}\right]\left[1 -\right.$$

$$e^{-\frac{1}{2}(\omega_{lpf}-\sqrt{{\omega_{lpf}}^2-\frac{4K_{PD}K_{VCO}}{N}})t}\Bigg] - \frac{1}{\omega_{lpf}+\sqrt{{\omega_{lpf}}^2-\frac{4K_{PD}K_{VCO}}{N}}}\Bigg[1 - e^{-\frac{1}{2}(\omega_{lpf}+\sqrt{{\omega_{lpf}}^2-\frac{4K_{PD}K_{VCO}}{N}})t}\Bigg]\Bigg] u(t)\Delta\omega \quad (36)$$

Equation 36 indicates two exponential terms decaying with time constants. Let's assume those time constants as$\tau_1$and τ_2Time constants can be written as,

$$\tau_1 = \left[\frac{1}{2}(\omega_{lpf} - \sqrt{{\omega_{lpf}}^2 - \frac{4K_{PD}K_{VCO}}{N}})\right]^{-1} \quad (37)$$

$$\tau_2 = \left[\frac{1}{2}(\omega_{lpf} + \sqrt{{\omega_{lpf}}^2 - \frac{4K_{PD}K_{VCO}}{N}})\right]^{-1} \quad (38)$$

Equations 37 and 38 prove that$\tau_1 > \tau_2$, hence settling time is determined by τ_1. Time constant τ_1 decreases with increasing value of$\frac{K_{PD}K_{VCO}}{N}$, the larger gain decreases the stability. It shows the trade-off between stability and settling time in type-1 PLL.

When${\omega_{lpf}}^2 - \frac{4K_{PD}K_{VCO}}{N} < 0$, two poles are complex, transient step response is given as

$$\omega_{out}(t) = \left[1 - e^{-\frac{1}{2}\omega_{lpf}t}\cos\left(\sqrt{\frac{4K_{PD}K_{VCO}}{N}) - {\omega_{lpf}}^2}\right) + \frac{\omega_{lpf}}{\sqrt{\frac{4K_{PD}K_{VCO}}{N}) - {\omega_{lpf}}^2}}\sin\left(\sqrt{\frac{4K_{PD}K_{VCO}}{N}) - {\omega_{lpf}}^2}\right)\right] Nu(t)\Delta\omega \quad (39)$$

If $\xi > 1$, the system is overdamped. Equation 39 shows that the step response contains a single exponential term with the time constant $2/\omega_{lpf}$. This is less than the time constant for a real pole case. For larger bandwidth, settling time is fast. Along with the trade-off between settling time, bandwidth and phase error, type-1 PLL suffers from the acquisition range. Type-2 PLL resolves these issues, also called charge pump PLL.

3.2. Type-2 PLL

Type-2 PLL consists of a second-order loop filter. The charge pump circuit is used to charge/ discharge the filter capacitor using MOS switches driven by PFD outputs UP and Down. This makes PLL a discrete system instead of a continuous system. The s-domain analysis is not possible for discrete systems. As per Gardner's limit, S-domain analysis is possible if loop bandwidth is less than one-tenth of the reference frequency.

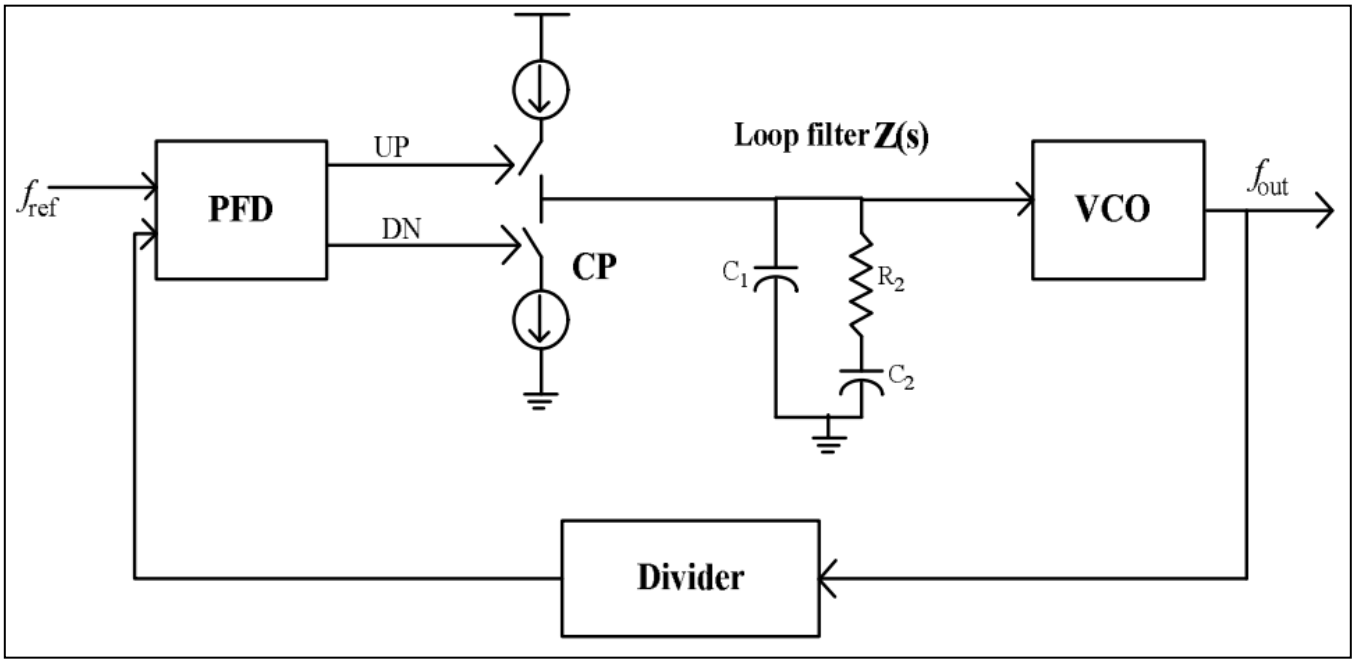

Fig. 3 Type-2 PLL

As shown in figure 3VCO acts as an integrator, and the combination of the charge pump, loop filter and PFD acts as another integrator. Hence there is an existence of two poles at the origin. This PLL is called a type-2 PLL. The open loop transfer function is written as,

$$H_o(S) = \frac{I_{cp}K_{VCO}}{2\pi N}\frac{L(S)}{S} \quad (40)$$

2nd order filter's transfer function is written as,

$$L(S) = \frac{1+sR_2C_2}{s^2R_2C_1C_2+s(C_1+C_2)} \quad (41)$$

Charge pump along with C_2 is responsible for the generation of a pole at zero frequency. To achieve a stable system R_2 along with C_2 generates zero. For suppression of high-frequency components on the VCO control line R_2 along with C_1 generates a pole. This pole must be greater than unity gain frequency to have a stable system. Pole and zero frequencies are given as

$$\omega_{p1} = \frac{C_2+C_1}{R_2C_2C_1} = \frac{1}{T_1} \quad (42)$$

$$\omega_{z1} = \frac{1}{R_2C_2} = \frac{1}{T_2} \quad (43)$$

Type-2 PLL's closed-loop transfer function is written as,

$$H_c(S) = \frac{I_{cp}K_{VCO}}{2\pi N(C_1+C_2)}\frac{1+sR_2C_2}{S^3\frac{R_2C_2C_1}{C_1+C_2}+S^2+S\frac{I_{cp}K_{VCO}R_2C_2}{2\pi N(C_1+C_2)}+\frac{I_{cp}K_{VCO}}{2\pi N(C_1+C_2)}} \quad (44)$$

As pole (ω_{p1}) is behind unity gain frequency, also C_2 is larger than C_1 the $H_c(S)$ is written as

$$H_c(S) = \frac{I_{cp}K_{VCO}}{2\pi NC_2}\frac{1+sR_2C_2}{S^2+S\frac{I_{cp}K_{VCO}R_2}{2\pi N}+\frac{I_{cp}K_{VCO}}{2\pi NC_2}} \quad (45)$$

Critical loop parameters are derived by comparing 45 with control theory's 2nd order negative feedback system.

$$\omega_n = \sqrt{\frac{I_{cp}K_{VCO}}{2\pi NC_2}} \quad (46)$$

$$\xi = \frac{R_2}{2}\sqrt{\frac{I_{cp}K_{VCO}C_2}{2\pi N}} \quad (47)$$

$$\phi_m = \tan^{-1}\left(\frac{\omega_c}{\omega_{z1}}\right) - tan^{-1}\left(\frac{\omega_c}{\omega_{p1}}\right) \quad (48)$$

ω_n is natural frequency, ξ is a damping factor, and phase margin is ϕ_m. Poles are calculated as,

$$S_{1,2} = \frac{1}{2}\left(-\frac{I_{cp}K_{VCO}R_2}{2\pi N} \pm \sqrt{\left(\frac{I_{cp}K_{VCO}R_2}{2\pi N}\right)^2 - \frac{4I_{cp}K_{VCO}}{2\pi NC_2}}\right) \quad (49)$$

Just like type-1 PLL, if poles are the complex system will have a larger settling time which means,

$$\left(\frac{I_{cp}K_{VCO}R_2}{2\pi N}\right)^2 - \frac{4I_{cp}K_{VCO}}{2\pi NC_2} < 0 \rightarrow \frac{I_{cp}K_{VCO}}{2\pi N} < \frac{4}{{R_2}^2C_2} \quad (50)$$

Transient response of system having complex poles is given as,

$$\omega_{out}(t) = \left[1 - e^{-\frac{1}{2}\left(\frac{I_{cp}K_{VCO}R_2}{2\pi N}\right)t}\right]\left[cos\left(\sqrt{\frac{4I_{cp}K_{VCO}}{2\pi NC_2} - \left(\frac{I_{cp}K_{VCO}R_2}{2\pi N}\right)^2}\,t + \frac{R_2C_2}{2\sqrt{\frac{4I_{cp}K_{VCO}}{2\pi NC_2} - \left(\frac{I_{cp}K_{VCO}R_2}{2\pi N}\right)^2}}\right) sin\left(\sqrt{\frac{4I_{cp}K_{VCO}}{2\pi NC_2} - \left(\frac{I_{cp}K_{VCO}R_2}{2\pi N}\right)^2}\right)t\right] Nu(t)\Delta\omega \quad (51)$$

The step response has only one exponential term with a time constant (τ).

$$\tau = \left(\frac{1}{2}\frac{I_{cp}K_{VCO}R_2}{2\pi N}\right)^2 \quad (52)$$

52show that by increasing $I_{cp}K_{VCO}$ Settling time decreases. It proves that trade-off does not exist in the selection of $I_{cp}K_{VCO}$. Hence type-2 PLL is chosen for high carrier frequency generation.

4. Implementation of PLL

The implementation of PLL is presented in this section. PLL building blocks, including phase frequency detector (PFD), a Charge pump (CP), Loop Filter (LPF), Voltage Controlled Oscillator(VCO) and feedback divider (FD), are implemented using cadence virtuoso 0.18 µm CMOS process. The PFD is implemented using two True Single Phase Clock (TSPC) D flip flops and a NAND gate in the feedback. To flow equal current through pull up and pull down networks width of PMOS is always maintained double that of NMOS. Here, the length of both NMOS and PMOS transistors is kept at 0.18 um, whereas the width of NMOS transistors is 4 um, and the width of PMOS transistors is *8 um*.

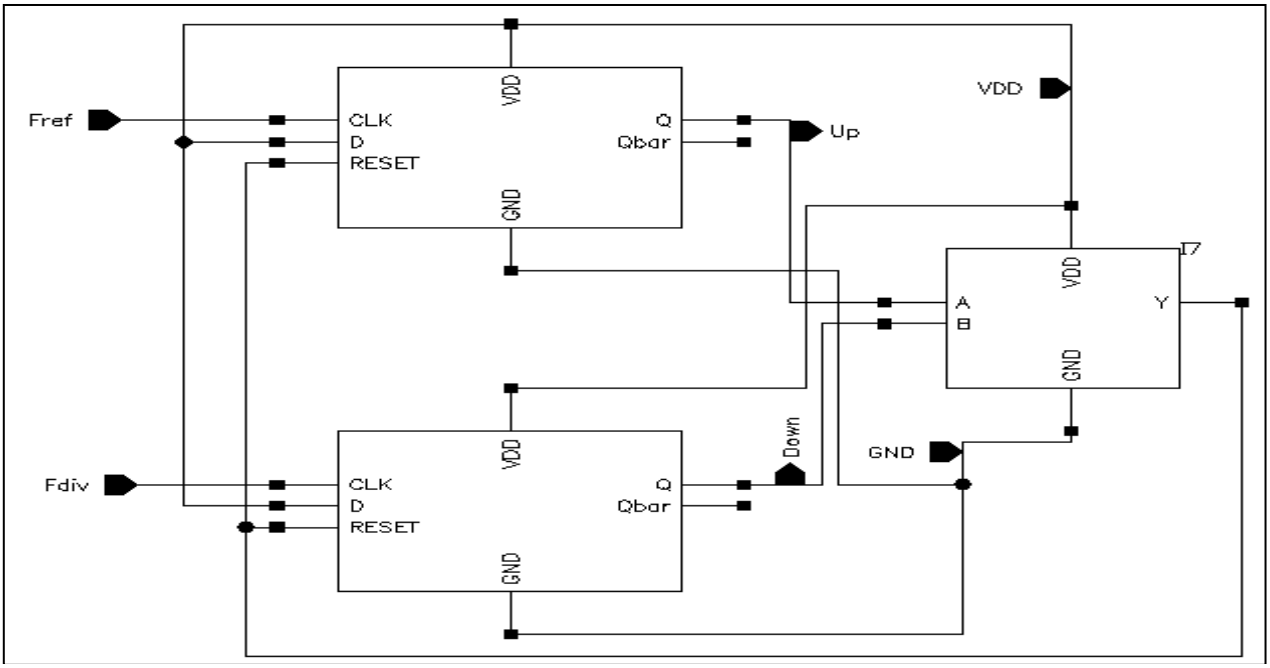

Fig. 4 PFD Schematic

The length of every MOSFET used in the charge pump circuit of figure 5 is kept at 0.18 *um*, and for reduction of current mismatch between up and down currents, widths are selected carefully. For n-channel MOSFETs named *NM0*, *NM1*, *NM2* and *NM3*, shown in figure 5, the width is calculated as 8 *um*. Similarly, for p-channel MOSFETs named *PM0*, *PM1*, *PM2* and *PM3*, width is calculated as 16 *um*, exactly double compared with n-channel MOSFET. The width of MOSFETs used in the OP-Amp design shown in figure 4.17 is kept as 8 *um*.

The filter bandwidth is a decade lower than the PLL input reference frequency. The ripple rejection capacitor is selected with a value 10 times larger than the holding capacitor, as shown in figure 6. The large size difference is maintained to keep filter characteristics unaffected.

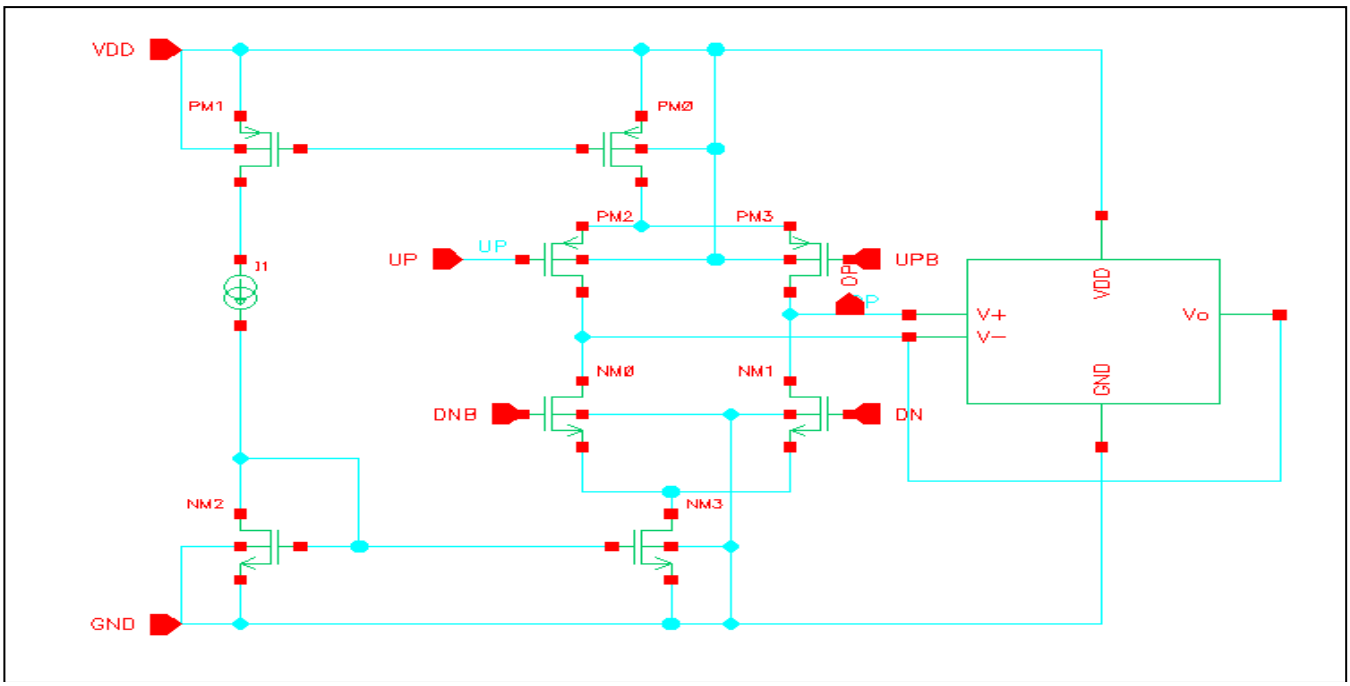

Fig. 5 Charge pump schematic

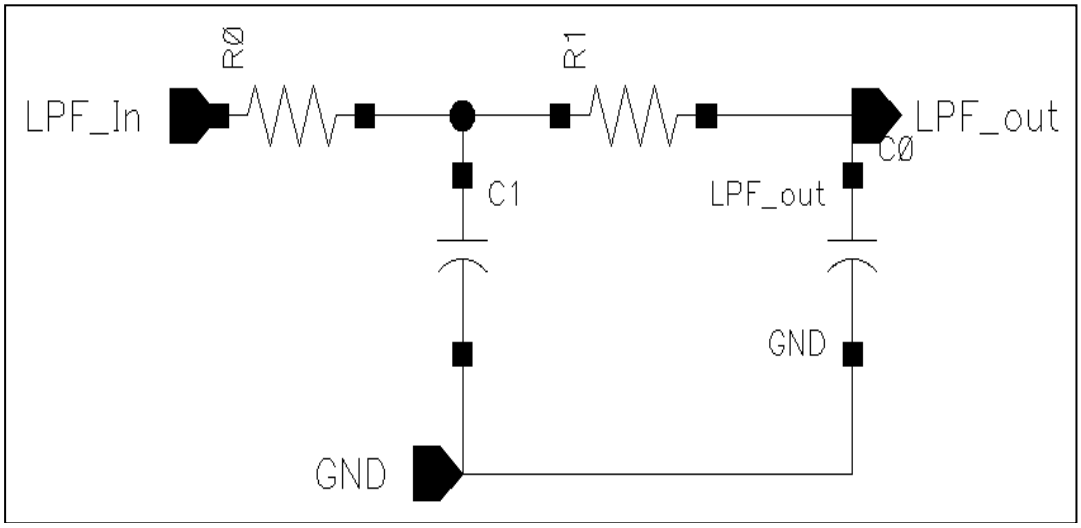

Fig. 6 Loop filter schematic

As shown in figure 7, the parasitic resistance generated by LC-tank is compensated using negative resistance (gm) generated by cross-coupled NMOS (NM1 and NM0) with bottom current biased. The active devices compensate for the energy loss in the tank. The energy loss must equal the energy supplied by the cross-coupled transistors to generate stable oscillations. The capacitor bank is implemented for coarse tuning, and the NMOS varactor is implemented for fine-tuning.
A chain of CML flip flops, as shown in figure 8, is implemented to achieve a programmable integer-N operation. These CML-based flip-flops help in saving size.

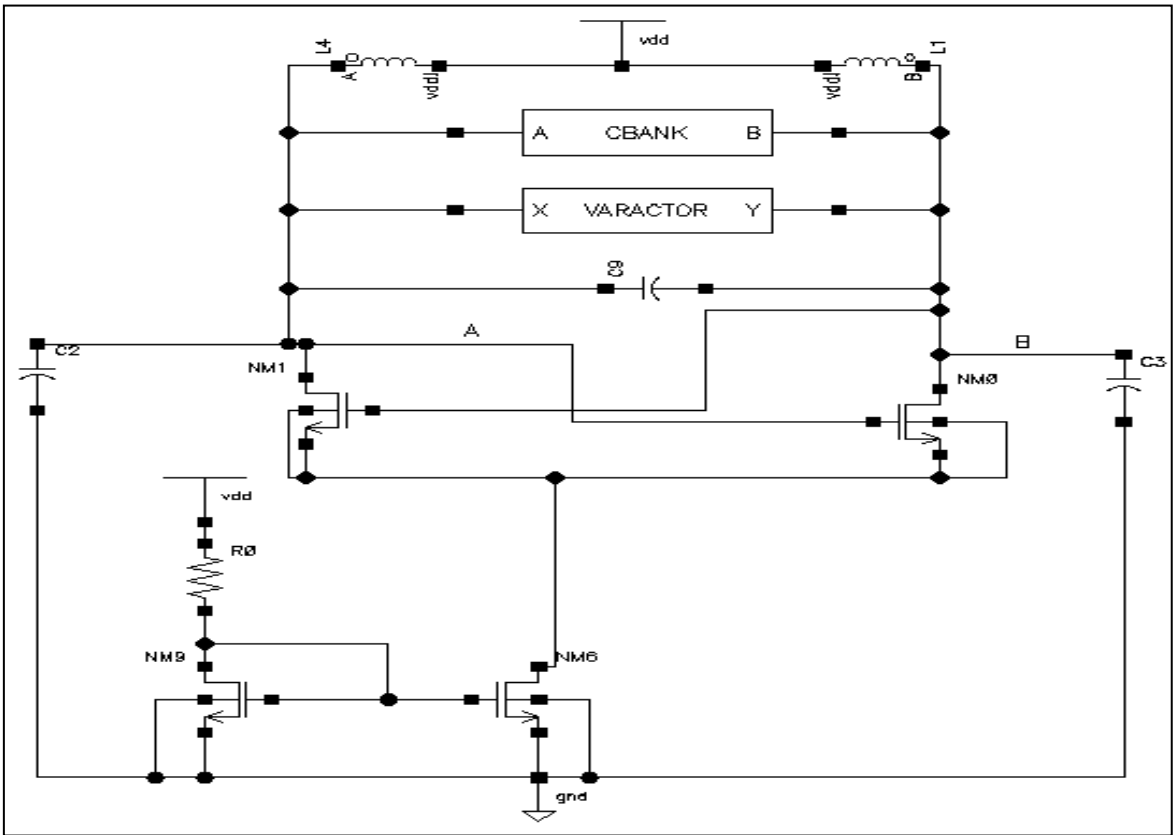

Fig. 7 VCO schematic

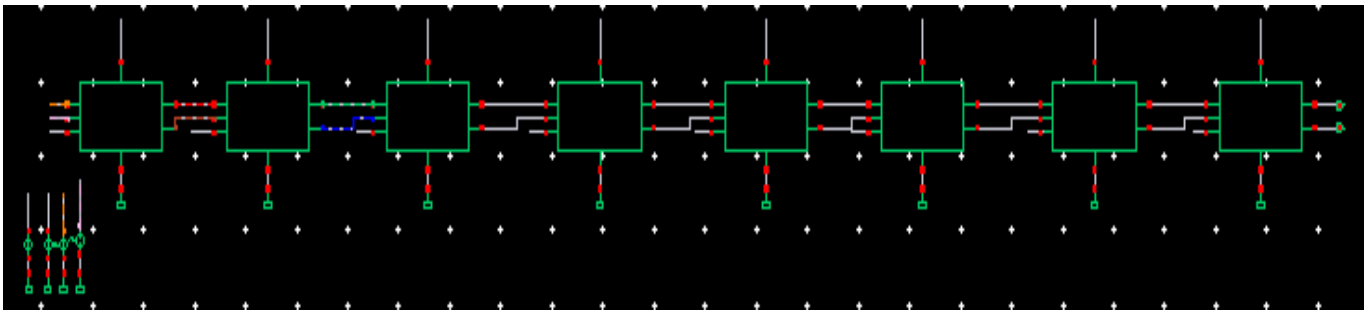

Fig. 8 Feedback divider schematic

A micrograph of the implemented PLL chip is presented in figure 9. The active area of the core is only0.076mm^2; LC VCO occupies 50% of the chip area. PLL output voltage swing is 2V, as presented in figure 10. Measurement results give phase noise of -122.84dBc/Hz and-114.60 dBc/Hz at 1MHz offset pre- layout and post layout, respectively, as shown in figures 11 and 12.

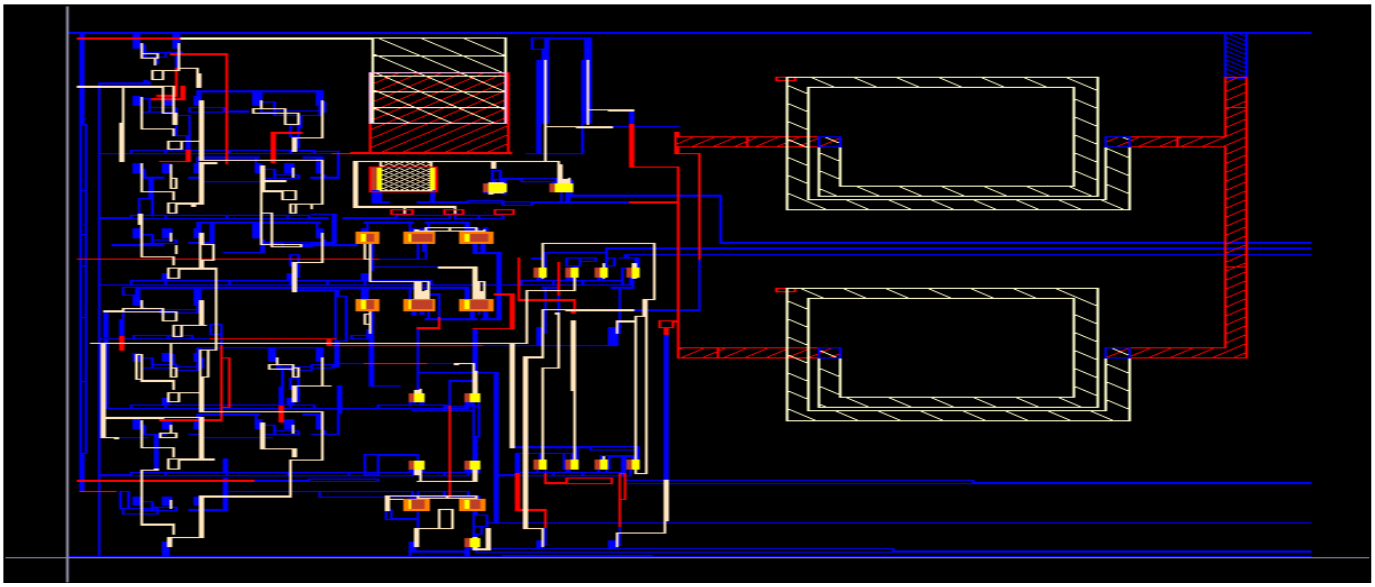

Fig. 9 PLL Layout

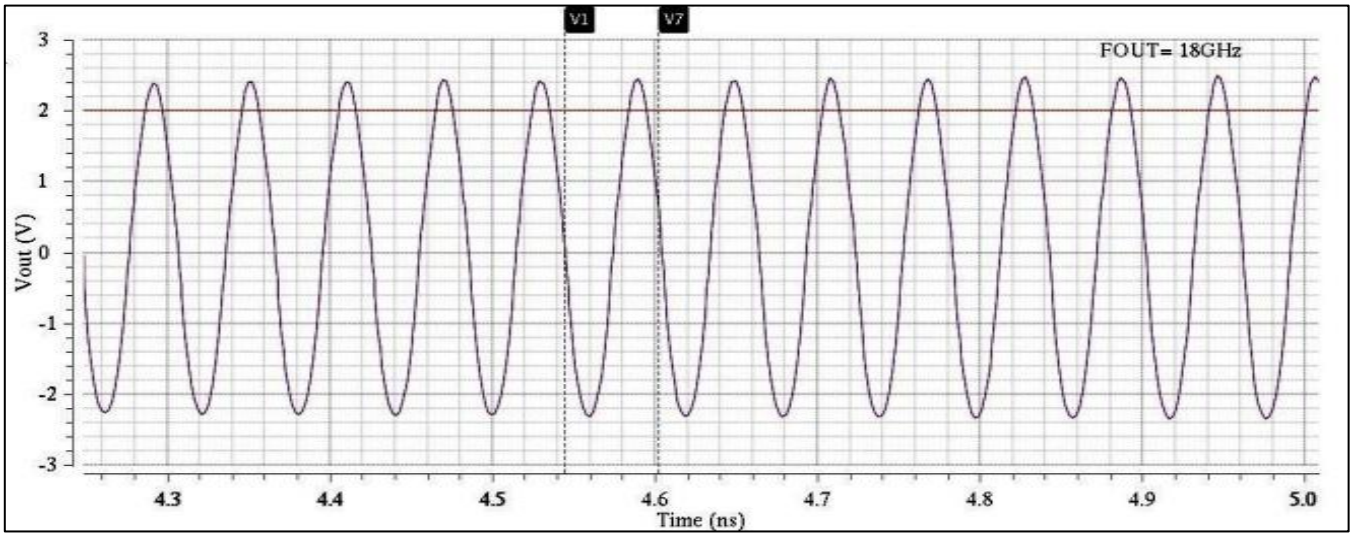

Fig. 10 PLL output waveform

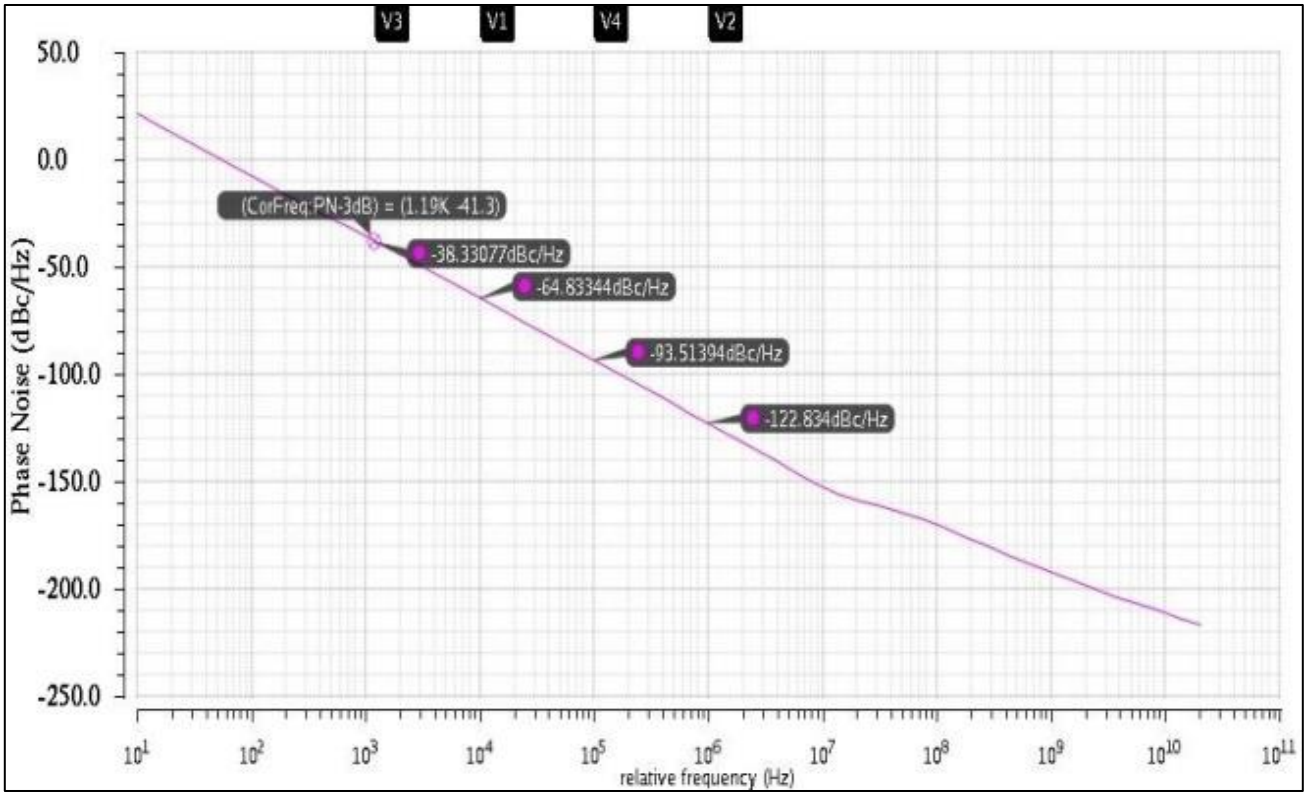

Fig. 11 PLL pre-layout phase noise performance

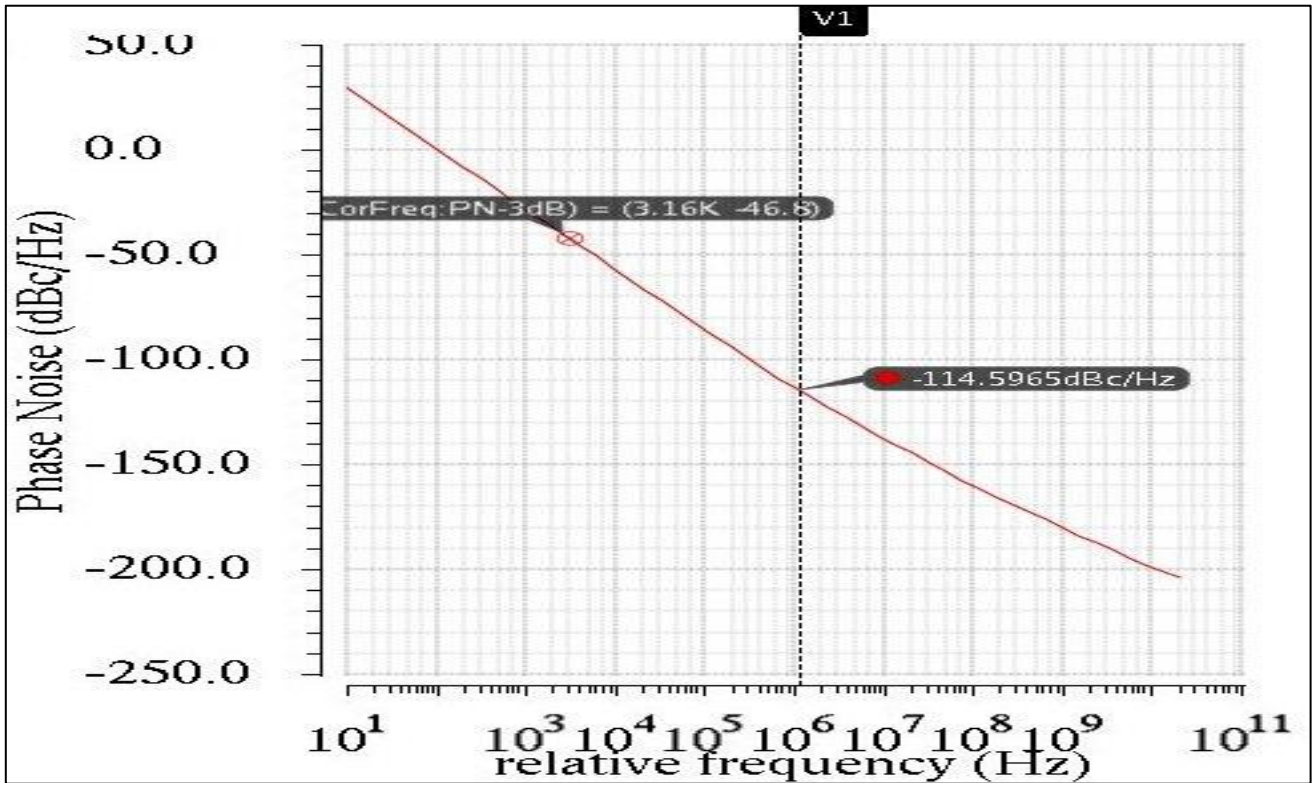

Fig. 12 PLL Post layout phase noise performance

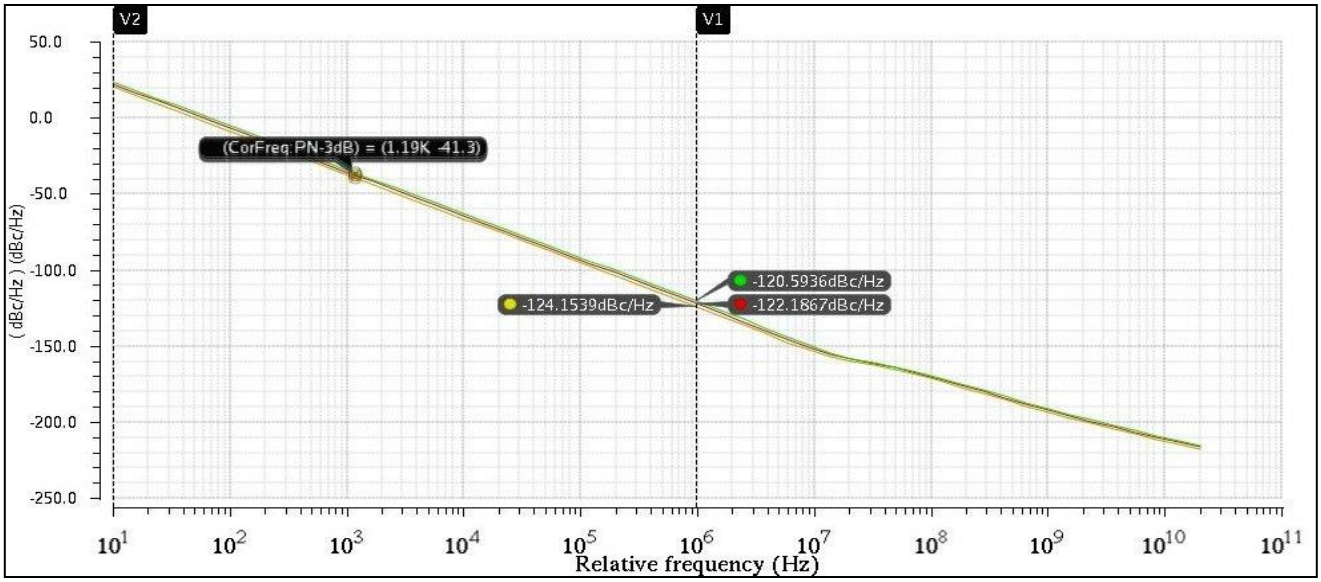

Fig. 13 PLL PVT Analysis

As presented in figure 13 implemented circuit gives a tuning range of 12GHz to 18 GHz, which covers the entire Ku band with an excellent phase noise of -64.83dBc/Hz, -93.51dBc/Hz and -122.83 dBc/Hz at an offset frequency of 10KHz, 100KHz and 1MHz respectively. The worst case phase noise of -120.59dBc/Hz and the best case phase noise of -124.19 @1MHz offset when running at 14.61 GHz oscillation frequency.

5. Measurement Results

PLL performance is compared with works intended for a similar frequency band. The performance of the implemented PLL is compared with the earlier work in table 1. Measurement results show the lowest reported phase noise at 1 MHz offset with an extremely wide tuning range.[3] Achieves phase noise comparable with this work, but the tuning range is half as compared to this. The chip area is not compared because, in previously implemented work, all elements are not integrated on the same chip. Novelty of this work is entire PLL elements are implemented on the same chip.

Table 1. PLL performance analysis

Ref.	Technology	Output Frequency (GHz)	VCO Type	Phase Noise (dBc/Hz @ 1MHz offset
[3]	0.12 µm	9.9-12.45	LC	-122
[6]	0.22 µm	5.8-7.2	DCO	-108
[14]	0.18 µm	13.9-15.6	Differential Colpitts	-103.8
[15]	0.13µm	11.37-14.8	LC	-112.5
This Work	0.18µm	12-18	LC	-122.83

6. Conclusion

This paper focuses on the design and implementation of ultra-low phase noise, wideband PLL frequency synthesizer on a single chip to be used in satellite transceivers. A Ku band (12 GHz to 18 GHz) novel fully integrated integer- N frequency synthesizer is implemented using 0.18μm CMOS process. Efforts have been put into size reduction and phase noise optimization by identifying in-band and out-of-band phase noise sources. The in-band phase noise is suppressed by loop bandwidth adjustment without degrading settling time. Out-of-band phase noise is suppressed by adjusting inductor Q in VCO.

Measurement results demonstrate that the size of the PLL implemented using 0.18 µm CMOS technology with 1.8V supply voltage is only 0.076mm^2, and LC VCO occupies 50% of the total chip area. Chip size can be reduced further by connecting VCO externally. The design gives a tuning range of 11GHz to 21 GHz, which occupies the Ku band along with a safety margin from both ends to compensate for the effect of parasitics. The analysis shows excellent phase noise of -64.83dBc/Hz, -93.51dBc/Hz and -122.83 dBc/Hz at an offset frequency of 10 kHz, 100 kHz and 1 MHz, respectively, from the carrier. The corner analysis gives the worst case phase noise of -120.59dBc/Hz and the best case phase noise of -124.19 @1MHz offset when running at 14.61 GHz oscillation frequency; this fulfils the requirement of satellite communication. The dead zone of the Phase Frequency Detector (PFD) is reduced to 1ps along with the negligible current mismatch ratio of 0.13% and a fabulous dynamic range of 0.3V to 0.9 V in the charge pump. The Lock-in range is 8.69 GHz, while the capture range is 5MHz.

References

[1] Albittar I.F and Dogan H, "A Novel Technique for Duty Cycle Correction for Reference Clocks in Frequency Synthesizers," *Elsevier Microelectronics Journal*, vol. 67, pp. 176–182, 2017. http://dx.doi.org/10.1016/j.mejo.2017.07.002.

[2] Choi Y.C, Seong Y.J, Yoo Y.J, Lee S.K, Lopez M.V, Yoo H.J, "Multi-Standard Hybrid PLL with Low Phase-Noise Characteristics for GSM/EDGE and LTE Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 10, pp. 3254-3264, 2015. https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7225192.

[3] Eric Wagner and Gabriel M. Rebeiz, "A Very Low Phase-Noise Transformer-Coupled Oscillator and PLL for 5G Communications in 0.12 μmSiGeBiCMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 4, 2020. DOI: 10.1109/TMTT.2019.2957372.

[4] G. Giustolisi, G. Palmisano, G. Palumbo, T. Segreto, "1.2-V CMOS Op-Amp with a Dynamically Biased Output Stage," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 632-636, 2000. https://ieeexplore.ieee.org/document/839923.

[5] Gao M.C, Bao K.Y, Huang F.Y, "A Broadband Low Phase Noise CMOS Voltage Controlled Oscillator for Ku Band," *IEEE International Conference on Integrated Circuits and Microsystems*, 2016. https://ieeexplore.ieee.org/document/7813575.

[6] In IEEE, J. Prinzie et al., "A Fast Locking 5.8–7.2-GHz Fractional-N Synthesizer with Sub-2-us Settling in 22-nm FDSOI," *Solid-State Circuits Letters*, vol. 3, pp. 546-549, 2020. Doi: 10.1109/LSSC.2020.3036122.

[7] Gonzalez-Diaz V.R, Sanchez-Gaspariano L.A, Muniz-Montero C, Alvarado-Pulido J.J, "Improving Linearity in MOS Varactor-based VCOs through the Output Quiescent Bias Point," *INTEGRATION the VLSI Journal*, vol. 55, pp. 274-280, 2016. http://dx.doi.org/10.1016/j.vlsi.2016.08.003.

[8] A. Sharkia, S. Aniruddhan, S. Mirabbasi and S. Shekhar, "A Compact, Voltage-Mode Type-I PLL with Gain-Boosted Saturated PFD and Synchronous Peak Tracking Loop Filter," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 1, pp. 43-53, 2019. Doi: 10.1109/TCSI.2018.2858197

[9] Lei Zhang, Zongmin Wang, Tieliang Zhang, et al., "An Improved Fast Acquisition Phase Frequency Detector for High-Speed Phase-Locked Loops", *AIP Conference Proceedings*, vol. 18, 2018.

[10] Chen Yingmei et al., "Low-Jitter PLL based on Symmetric Phase-Frequency Detector Technique", *Analog IntegrCirc Sig Process*, 2010.

[11] Pawar S.N and Mane P.B, "Wideband PLL Frequency Synthesizer: A Survey," *International Conference on Advances in Computing, Communication and Control (ICAC3)*, 2017. https://ieeexplore.ieee.org/document/8318773.

[12] Scotti G, Bellizia D, Trifiletti A, Palumbo G, "Design of Low-Voltage High-Speed CML D-Latches in Nanometer CMOS Technologies," *IEEE Transactions On Large-Scale Integration (VLSI) Systems*, vol. 25, no. 12, pp. 1-12, 2017. https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8048001.

[13] Sung Sik Park et al., "Phase Frequency Detector and Charge Pump for Low Jitter PLL Applications", *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 8, no. 6, 2018.

[14] Y. Peng and L. Lu, "A 16-GHz Triple-Modulus Phase-Switching Prescaler and its Application to a 15-GHz Frequency Synthesizer in 0.18-μm CMOS," *in IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 1, pp. 44-51, 2007. Doi: 10.1109/TMTT.2006.886908.

[15] Zhang Y, Tang X, Wei Z, Bao K, Jiang N, "A Ku-Band Fractional-*N* Frequency Synthesizer with Adaptive Loop Band Width Control," *Electronics*, vol. 10, pp. 109, 2021. http://doi.org/10.3390/electronics10020109

[16] Mane P B and Pawar S N, "An Ultra-Low Current Mismatch Charge Pumpand Loop Filter in 0.18um CMOS Process for Low Spur PLL Applications", *International Journal of Engineering Trends and Technology*, vol. 69, no. 6, pp. 14-24, 2021.

[17] Zhu W, Yang H, Gao T, Liu F, Yin T, Zang D, Zang H, "A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler," *IEEE Transactions on Large-Scale Integration (VLSI) Systems*, vol. 23, no. 1, pp. 194-197, 2015. https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6734682.

[18] Vaishali and R. K. Sharma, "An Improved Dynamic Range ChargePump with Reduced Current Mismatch for PLL Applications," *Second International Conference on Intelligent Computing and Control Systems*, Madurai, India, 2018. Doi: 10.1109/ICCONS.2018.8663212.

[19] S. Jandhyala and S. Tapse, "A 1.3V–1.8V Configurable Phase-Locked Loop with an Adaptive Charge Pump," *IEEE Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER)*, pp. 138-140, 2016. Doi: 10.1109/DISCOVER.2016.7806236.

[20] A. G. Amer, S. A. Ibrahim and H. F. Ragai, "A Novel Current Steering Charge Pump with Low Current Mismatch and Variation," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1666-1669, 2016. Doi: 10.1109/ISCAS.2016.7538887.

[21] Chih-Ming Hung and K. K. O, "A Fully Integrated 1.5-V 5.5-Ghz CMOS Phase-Locked Loop," in IEEE Journal of Solid-State Circuits, vol. 37, no. 4, pp. 521-525, 2002. Doi: 10.1109/4.991390.

[22] R. A. Baki and M. N. El-Gamal, "*A New CMOS Charge Pumpfor Low-Voltage (1V) High-Speed PLL Applications, Circuits and Systems*," ISCAS '03, Proceedings of the 2003 International Symposium, vol. 1, pp. I-657-I-660, 2003.

[23] J. Gupta, A. Sangal and H. Verma, "High-Speed CMOS Charge Pump Circuit for PLL Applications using 90nm CMOS Technology," *World Congress on Information and Communication Technologies*, pp. 346-349, 2011. Doi: 10.1109/WICT.2011.6141270.

[24] Zou Q, Ma K, Yeo K.S, Lim W.M, “Design of a Ku-Band Low-Phase-Noise VCO using the Dual LC Tanks,” *IEEE Transactions on Circuits and Systems—Ii: Express Briefs*, vol. 59, no. 5, pp. 262-266, 2012. https://ieeexplore.ieee.org/document/6189056

[25] Z. Zhang, H. Djahanshahi, C. Gu, M. Patel and L. Chen, "Single-Event Effects Characterization of LC-VCO PLLs in a 28-nm CMOS Technology", *in IEEE Transactions on Nuclear Science*, vol. 67, no. 9, pp. 2042-2050, 2020. Doi: 10.1109/TNS.2020.3008142.

[26] S. Ji, Y. Zhao, W. Xu, N. Yan and H. Min, "A Novel Charge Pump with Ultra-Low Current Mismatch and Variation for PLL," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain, pp. 1-4, 2020. Doi: 10.1109/ISCAS45731.2020.9180830.

[27] M. Leoncini, A. Bonfanti, S. Levantino and A. L. Lacaita, "Efficient Behavioral Simulation of Charge-Pump Phase-Locked Loops," *in IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 6, pp. 1968-1980, 2018. Doi: 10.1109/TCSI.2017.2767280.

[28] C. Ko, T. Kuan, R. Shen and C. Chang, "A 7-nm FinFET CMOS PLL With 388-fs Jitter and −80-dBc Reference Spur Featuring a Track-and-Hold Charge Pump and Automatic Loop Gain Control," *in IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1043-1050, 2020. Doi: 10.1109/JSSC.2019.2959735.

[29] A. Homayoun and B. Razavi, "On the Stability of Charge-Pump Phase-Locked Loops," *in IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 6, pp. 741-750, 2016. Doi: 10.1109/TCSI.2016.2537823.

[30] C. C. Boon, M. V. Krishna, M. A. Do, K. S. Yeo, A. V. Do and T. S. Wong, "A 1.2 V 2.4 GHz Low Spur CMOS PLL Synthesizer with a Gain Boosted Charge Pump for a Batteryless Transceiver," *IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Singapore, pp. 222-224, 2012. Doi: 10.1109/RFIT.2012.6401667.

[31] D. Liao, Y. Zhang, F. F. Dai, Z. Chen and Y. Wang, "An mm-Wave Synthesizer with Robust Locking Reference-Sampling PLL and Wide-Range Injection-Locked VCO," *in IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 536-546, 2020. Doi: 10.1109/JSSC.2019.2959513.

[32] T. Wu, P. K. Hanumolu, K. Mayaram and U. Moon, "Method for a Constant Loop Bandwidth in LC-VCO PLL Frequency Synthesizers," *in IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 427-435, 2009. Doi: 10.1109/JSSC.2008.2010792.

[33] S. N. Pawar and P. B. Mane, "Design and Implementation of KU Band LC-VCO using 90nm CMOS Process," *International Conference on Smart Electronics and Communication (ICOSEC)*, Trichy, India, pp. 1234-1238, 2020. Doi: 10.1109/ICOSEC49089.2020.9215283.

[34] X. Liu and H. C. Luong, "A Fully Integrated 0.27-THz Injection-Locked Frequency Synthesizer with Frequency-Tracking Loop in 65-nm CMOS," *in IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1051-1063, 2020. Doi: 10.1109/JSSC.2019.2954232.

Bibliography

Dr. Shobha N. Pawar received her BE (E&TC) degree from the University of Pune, Maharashtra, India in 2007, ME (E&TC - Microwaves) from Savitribai Phule Pune University, Pune in 2012 and Ph.D. from Savitribai Phule Pune University, Pune in 2022. She has teaching experience of 13years and research experience of 1.5 years; currently, she is associated with AISSMS Institute of Information Technology, Pune, as an Assistant Professor in Electronics and Telecommunication Engineering. She has published papers in 20 international journals and presented Papers in 6 international conferences. She was principal Investigator of ISRO-UOP sponsored research project. She is A life member of ISTE, IETE and member of IEEE.

Dr. Pradeep B. Mane received his BE (E&TC) and ME (E&TC) degree from Government College of Engineering Pune, India and P.hD from Bharati Vidyapeeth University, Pune. He worked in Philips India ltd. for 3 years, 15 years in Bharati Vidyapeeth COE Pune and currently working as a Principal in AISSMS’s Institute of Information Technology, Pune, affiliated with Savitribai Phule Pune University. He was a member of the BOS for Electronics faculty in Bharati Vidyapith University and Savitribai Phule Pune University. He has co-authored 6 books for engineering courses with Wiley and Technova publications in the field of Radio and TV engineering and Computer networks. He has published 50 papers in national, International conferences and seminars. He has 47 Publications in international journals. He is a regular reviewer For Springer Wireless Personal Communication journal. His Area of interest is wired, wireless communication and Computer networks. He was CO-PI for ISRO-UOP research Grant. He is a fellow of IEI, IETE and a member of IEEE, ISA, IJERIA and ISTE. He has received national awards for Best Engineering College Principal for the year 2017 from Bharatiya Vidya Bhavan(ISTE) and Computer Society of India (CSI). He is recognized as a Ph.D Guide of Savitribai Phule Pune University and Bharati Vidyapeeth deemed universities in Electronics engineering. Four students have completed Ph.D. Under his guidance and eight students are currently working Under his guidance.

Mr. Milind P Gajare received his BE (E&TC) degree from North Maharashtra Univesity, Maharashtra, India, in 2002 and ME (E&TC –VLSI and Embedded Systems) from Savitribai Phule Pune University, Pune, in 2017. Currently, he is pursuing a Ph.D from AISSMS's Institute of Information Technology affiliated with SavitribaiPhule Pune University, Pune. He has teaching experience of 17 years and research experience of 3.5 years; currently, he is associated with AISSMS Institute of Information Technology, Pune, as an Assistant Professor in Electronics and Telecommunication Engineering. He has published papers in 20 international journals and presented Papers in 2 international conferences. He is a life member of ISTE and IETE.