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Original Article

Optimization of Retention Time in 3T DRAM using Anti-Body Bias Technique in Nanoscale Technology

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Abstract *- Retention time is responsible for data storage operation in semiconductor memories. But it depends upon the charge retention capacity of the storage capacitor. During the implementation of low-power electronic gadgets, small device geometry, minimum operating voltage and optimization in parameters circuit designers face the issues of leakage parameters to great extent. As the demand for high-density storage memories increases day by day moore's law supports more number of transistor in the nanometer area on the silicon wafer. Scaling plays a crucial role in small device geometry in nanometer scale cmos technology but it has some limitations over it. In this paper leakage parameters, comparative analysis using cmos, finfet and anti-body bias technique for retention time improvement is carried out. 3T DRAM having an inverter circuit with proper biasing at the substrate terminal offer minimized leakage parameter and improvement in retention time is observed. Cmos, finfet and anti-body bias technique in 3T DRAM is implemented with 90nm technology using a cadence tool. In supply voltage variation leakage current reduction is observed at 75% in the finfet technique and 82% observed in the anti-body bias technique. In capacitance value variation leakage current reduction is observed at 94% in the finfet technique and 96% observed in the anti-body bias technique. Anti-body bias technique offers excellent results in comparison with cmos and finfet technology is examined.*

Keywords *- Anti-body bias, Cmos, Finfet, Leakage current, Refresh frequency, and Retention time.*

1. Introduction

Nowadays, In the electronics era due to the invention and scaling of mos devices integrated circuit technology enhances very rapidly day by day. Retention time plays a primary and prominent role in data storage operation in semiconductor memories. There are various leakage sources or paths in mos devices due to which the probability of loss of information or data may occur. To preclude loss of information and improve the retention time several leakage reduction techniques were proposed. Scaling in mos devices offer minimum area, and compact device size and improves the density of semiconductor memories in electronic appliances. As the device size shrinks down, The performance of mos devices is affected by the various leakage parameters VLSI circuit designers have the biggest challenges for the implementation of compact, low-power and high-performance electronic gadgets. DRAM was implemented with various previous circuit techniques, Also 3T DRAM was implemented with cmos technology but it has certain limitations over existing leakage reduction techniques. To overcome the leakage parameters issues and to improve performance in terms of retention time(T_h) and refresh frequency($F_{refresh}$) in 3T DRAM anti-body bias technique is proposed.

Finfet technology is an improved form of cmos technology for the same working principle but improved for leakage minimization in mos transistor devices. Similarly for more or additional improvement in retention time and minimize leakage parameters anti-body bias leakage reduction technique is proposed. In this method, the bias voltage is applied to the substrate terminal of the mos device through an inverter-based circuit. In both the substrate bias technique i.e. FBB and RBB slight increases in the threshold voltage were observed. Therefore by applying proper FBB and RBB the leakage parameters can be controlled. By applying proper biasing in FBB and RBB leakage parameters can be controlled to great extent and helps to improve the retention time in dynamic random access memory.

The key findings in this paper are

- ✓ The leakage parameters are characterized, analyzed and computed by Cmos, Finfet and Anti-body bias by parametric variation using leakage reduction techniques.
- ✓ Retention time computation is carried out with cmos, finfet and anti-body bias techniques.
- ✓ Compute the refresh frequency with all techniques and how it inversely varies with retention time is examined.
- ✓ Anti-body bias technique provides excellent results as compared to the cmos and finfet techniques that were proposed.

2. Literature Review

The field of electronics plays a very important role in the era of electronic appliances. In several electronic gadgets, the data is stored in semiconductor memory chips. This memory storage capacity depends upon the device used for which type of application and vice versa. Dynamic random access memory (DRAM) is the leading or popular storage device choice for the circuit designer in electronic gadgets. The data is stored on dram in the form of an electronic charge over it. The structure of the basic dram cell has mos transistor, and storage capacitor and it is controlled by a word line(W_L) and bit line(B_L) respectively. The controlling action in the dram cell maintains by a word line and bit line. Due to several types of leakages in mos transistor offer loss of stored information or data from storage capacitor. To prevent this destructive action of loss of information refresh is required in the memory cell after some interval of time. But regularly refresh operation deteriorates the system performance adversely. To minimize the issue related to leakage parameters and refresh operation anti-body bias technique is proposed to expand the performance of dynamic random access memories.

Leakage parameters in mos transistors are majorly responsible for performance degradation. In mos devices off-state leakage current offer tremendous power dissipation. In this paper implementation of 3T DRAM by anti-body bias technique is proposed for the reduction of leakage parameters. Anti-body bias leakage reduction techniques in mos devices overcome the issues related to finfet technology to great extent.[1] In this paper reliability, variability and soft error rate issues are examined by the implementation of a dram with planar mosfet, finfet and III-IV mos devices. After the comparison of results from various circuits, finfet technologies provide excellent results overall techniques.[2] Previously L1 memory cache is designed with six mos transistor to overcome the issues related to the same it is replaced by a 3T1D cell for device variability.[3] High-density dynamic random access memory is needed for data storing electronic devices. A concept of the charge injection device implemented for high-density memories having a minimum size of mos transistor was proposed. The implemented mos transistor required the least area in comparison with the traditional mos transistor.[4] Short channel effect and leakage current affect the performance of the integrated circuit or small electronic circuit implemented by cmos circuit. Here the leakage current contributes to maximum power dissipation in the integrated circuit was implemented by cmos technology. [5] The carbon nanotube is used instead of traditional mos device for investigation of delay time and leakage parameters. For the implementation of 3T DRAM and 4T DRAM, it has been observed that 3T DRAM has minimum leakage parameters i.e. leakage current and leakage power. But delay time is more in 3T DRAM as in comparison with 4T DRAM suggested.[6] 3T1D and modified 3T1D were designed for leakage parameter analysis. Access time and power consumption parameters were examined with 3T1D DRAM and results were compared. The retention time parameter slightly improved in the modified 3T1D DRAM as compared to the traditional model was compared. [7] Integrated circuits were implemented with cmos, soi and finfet technology for comparative analysis of various leakage parameters and finfet technology having minimum leakage parameters.[8] 3T DRAM and 4T DRAM were implemented with different nanometer regimes for power dissipation analysis. In mos devices, the main cause of power dissipation (P_d) was off-state (I_{off}) leakage current. During comparison with variation in technology, At 45nm technology average power dissipation is minimum in 3T DRAM as compared to 4T DRAM were examined and comparative analysis was carried out.[9] For planar mos devices, finfet is the best option while device size is scaled down. In double gate finfet technology (DG-Finfet) gate has more control over the source and drain. In DG-Finfet technology leakage current intensity is minimized compared to cmos technology was examined.[10] In static random access memory, data stability is a more important parameter. High-density memory arrays occupied in small silicon wafers were the primary source of leakages in mos devices. Active and standby power reduction is achieved through independent gate finfet(IGF) for improvement in data stability and memory density.[11] Device variability is a major issue in semiconductor devices as it scaled down more and more. For device variability parameters the finfet technology offers excellent results as compared to SOI and cmos technology.[12] Retention or holding time(T_h) and refresh frequency($F_{refresh}$) are inverses inter related parameters considered for advancing the performance in DRAM memory cell structure. By parametric variation in dynamic random access memories leakage parameters performance was examined. The leakage parameter adversely affects the retention time of DRAM memories were observed.[13] Basically, in mos devices, the performance was degraded due to the effect of leakage parameters. Due to numerous leakage sources in mos transistor leakage parameters were calculated by parametric variation. Increase in the capacitance value the leakage parameters minimized to great extent were observed.[14] When the $V_{gs} < V_{th}$ sub-threshold current contribute to leakage current parameter. Variation in dielectric constant and difference between top and flat band voltage determine the sub-threshold characteristic of mos devices.[15] In modern electronic gadgets low power, small device geometry and maximum efficiency trends more popular day by day. By adjusting the threshold voltage by variable doping profile the low-power device implementation was proposed.[16] The parasitic effect plays a prominent role in VLSI circuits and it affects the system performance observed. To overcome the issues related to parasitic effects different doping profiles in mosfet were proposed.[17] In this paper domino logic in finfet technology is proposed using on-off logic. Due to this logic, sub-threshold leakage currents were minimized was

examined.SG and LP modes were considered for input and seen the effect of leakage current by variation in temperature.[18] In this paper independent gate finfet circuits were implemented with the dynamic adjustment of threshold voltage proposed. As per the operating frequency and mode threshold voltage were adjusted to minimize the leakage parameter.[19] To minimized the leakage power and improvement of noise immunity and speed parameter in the domino logic integrated circuit variable voltage keeper technique was proposed.[20] Sleep switch transistor techniques were proposed for the reduction of sub-threshold leakage current (I_{off}) to large extent having more control during operation.[27] As the device is reduced by the scaling technique, oxide thickness reduction and gate tunneling path contribute more to the device leakage current. In this paper variations in technology affect the transistor length and how it varies the gate oxide thickness was proposed. Similarly, the transistor stacking technique in variable oxide thickness and how it effectively minimized leakage parameters were seen.[22] Scaling makes it possible for the reduction in threshold voltage correspondingly there is an increase in sub-threshold leakage current. The lector transistor technique minimized the dynamic power dissipation in cmos devices.[23] In this paper sources of leakages in mos transistor and leakage reduction techniques were proposed as per the various parameters and controlling circuitry with them. Large leakage current majorly contributes to power dissipation in cmos devices. Reduction in threshold voltage, Gate oxide thickness and channel length affect the system performance and help to increase the leakage current were proposed.[24] Super cut-off cmos techniques were proposed for high speed and low leakage current in integrated circuit technology.[25] 3T DRAM is implemented with double gate finfet technology for the reduction of leakage parameters. Here comparative analyses were carried out with cmos and double gate finfet technology. The Finfet technique provides better retention time and improved results as compared to the traditional cmos technology proposed.[26]

3. Three Transistor Dynamic Random Access Cell And Performance Measuring Parameters

3.1 Basic Structure of Three Transistor DRAM Cell

DRAM cell with three transistors i.e. Mosfet M_1, M_2 and M_3 respectively. The memory cell structures are controlled by read(R) and write(W) signals. C_1 and C_2 are precharge capacitors and C_s is the storage capacitor used for charge storage operation in forms of 0 or 1.

The switching action i.e. ON and OFF in mos devices is controlled by the read and write line respectively. There are three capacitors C_1, C_2 and C_s. Precharging operation is controlled by C_1 and C_2 capacitors. Depending on the switching action in mos transistors data is kept at storage capacitor C_s in form of a charge over it.

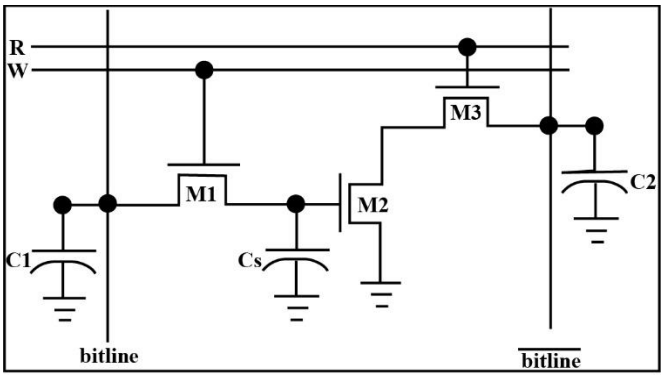

Fig. 1 Basic Three Transistor DRAM Cell

In data, input operation writes line=logic 1, read line=logic 0, transistor M_1=on and transistor M_2=M_3=off, and C_1 is a precharge capacitor to V_{dd}. During data storage operation the maximum voltage that appears across the storage capacitor is 'V_{dd}-V_{th}'. When there is no charge on the storage capacitor the voltage across the storage capacitor is logic 0 i.e. 0V.

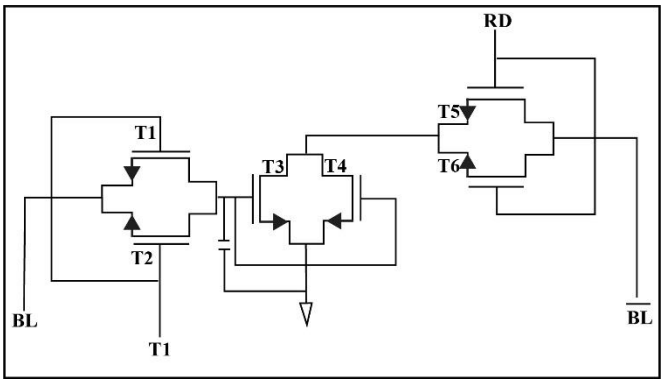

Fig. 2 Three Transistor DRAM with Double gate finfet Technique

During a read operation, the control line i.e. Read line= logic 1 and Write line =logic 0, transistor M_3=on and M_1=off, the charge on the precharge capacitor C_2 become V_{dd}. In this condition, the voltage that appears across the storage capacitor is maximum i.e.V_{dd}-V_{th}. This maximum voltage 'V_{dd}-V_{th}' turns on the mos transistor M_2. If mos transistor M_2 and M_3 both turns on the voltage across precharge capacitor C_2 start reducing, Hence the voltage measured at the bitline bar is logic 0 and it is measured by a sense amplifier (SA) and it signifies logic 1.

The voltage that appears across the storage capacitor is logic 0 i.e 0 Volt, It will turn off mos transistor M_2. In this case, if M_2=off and M_3=on the voltage appears across the precharge capacitor($C_{precharge}$) i.e.C_2 is maximum i.e. Vdd. Therefore the voltage that appears at the bit line bar is logic 1 i.e.V_{dd} and it measures by a sense amplifier (SA) and it signifies logic 0.

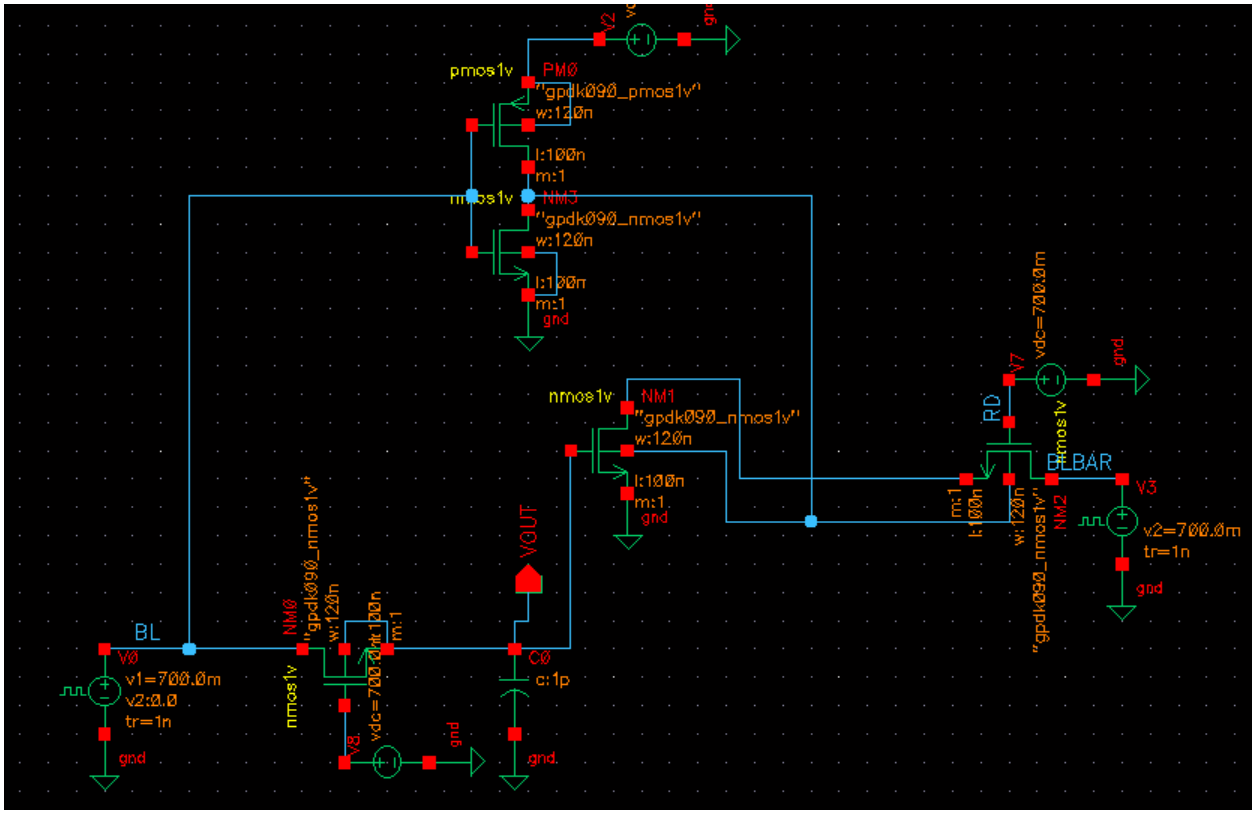

Fig. 3 Three Transistor DRAM with anti-body bias technique

3.2 Performance Measurement Parameters

The primary and principle aim of the implementation of three transistors is dynamic random access memory with leakage reduction techniques for minimization of leakage parameters and optimization of retention time in semiconductor memories. Leakage parameters in mos devices adversely affect the system performance and for minimization, it required additional circuitry. Additional use of leakage reduction circuitry there may be the possibility of static power dissipation. The static power dissipation depends on the leakage current due to the minority charge carrier. The mathematical expression for leakage currents with the condition and retention time is mathematically expressed as follows.

3.2.1 Sub-threshold Leakage Current

Sub-threshold leakage current occurs when the gate to source voltage (V_{gs}) is minimum as compared to the threshold voltage(V_{th}) of the mos transistor. When the bias voltage is less as compared to the threshold voltage operating region for the mos transistor is a weak inversion region and in this region mos device is in an off state. When the mos device is in an off state there is a minimum amount of current flowing due to the minority charge carrier responsible for leakage current in the mos transistor. The leakage path inside the mos transistor is responsible for the charge over the leak through this path. The mathematical representation of sub-threshold leakage ($I_{subthreshold}$) current is expressed as follows

$$I_{subthreshold}=I_o e^{(Vgs-Vth)/(nVT)}[\ 1- e^{-(Vds/VT)}\ ] \ldots\ldots(1)$$

Where,

V_{th} = Threshold voltage,
V_{ds} = Drain to source voltage,
V_{gs} = Gate to source voltage,
C_{ox} = Gate oxide capacitance,
μ_o = Carrier mobility,
n = Sub-threshold swing coefficient,
L = Transistor Length,
W = Transistor Width.

3.2.2 Leakage Power

Scaling plays a crucial role in restructuring device geometry in mos transistors. Restructuring or lay-outing in mos structure design offers minimum device size. Minimum device size may responsible for power dissipation. Power dissipation issue arises in mos device in the minimum area due to scaling and it contributes to leakage power. The mathematical leakage power can be expressed as

$$P_{LeakPower} = I_{LeakCurrent} * V_{SupplyVoltage} \ldots\ldots\ldots(2)$$

Where,

$P_{LeakPower}$ = Leakage Power,
$I_{LeakCurrent}$ = Leakage Current,
$V_{SupplyVoltage}$ = DC Power Supply.

3.2.3 Retention Time (T_h)

The parameter retention time is responsible for data storage operation in semiconductor memory. It is the data holding capacity of the dram cell. The maximum period at which the cell might maintain a sufficient voltage to be measured is logic 1. The holding time or retention time(T_h) can be expressed as

$$\text{Retention Time} = T_h = \Delta t = [C_S/I_L] * \Delta V_S \ldots\ldots\ldots (3)$$

Where,

$C_{Storage}$= Charge Storing Capacitor

I_{Leak} = Leak Current in mos device

Changes in time represent Δt and changes in supply voltage represent ΔV_S.

By using a large value of storage capacitance leakage current can be minimized correspondingly the retention time(Th) improvement is possible. But with the use of a large value of storage capacitor in a dynamic memory array, there may be possibilities of parasites.

3.2.4. Refresh Frequency ($F_{Refresh}$)

Refresh rate is an important parameter in semiconductor memory. The refresh rate is directly proportional to refresh frequency. In dynamic memory due to charge leakage issue possibility of information loss increases to a large extent. To avoid this loss of information refresh is important in dynamic random access memory. Refresh frequency is inversely proportional to retention time and vice versa. As retention time increases, refresh frequency decreases and vice versa. For proper operation of dram, avoiding the loss of information and improvements in retention time various leakage reduction techniques were proposed. Mathematically refresh frequency ($F_{refresh}$) can be expressed as

$$F_{Refresh} = [1/2T_h] \ldots\ldots\ldots\ldots\ldots (4)$$

Where

T_h=Data holding time

3.3. Three Transistor Schematic Diagram

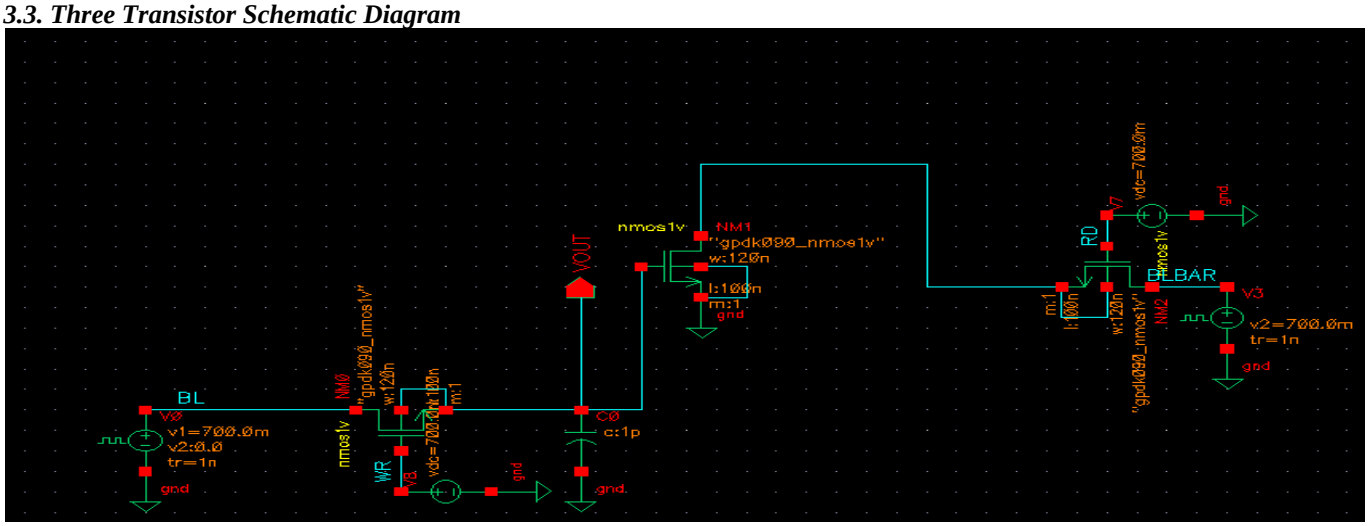

Fig. 4 Three Transistor DRAM Implementation

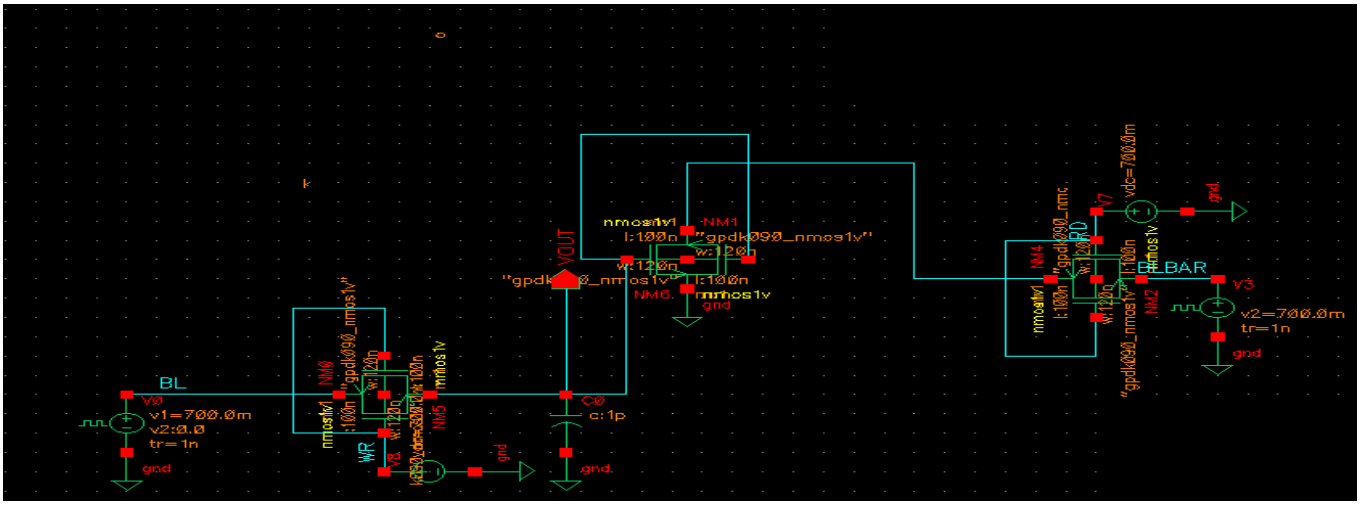

Fig. 5 Three Transistor DRAM with DG-Finfet technique Implementation

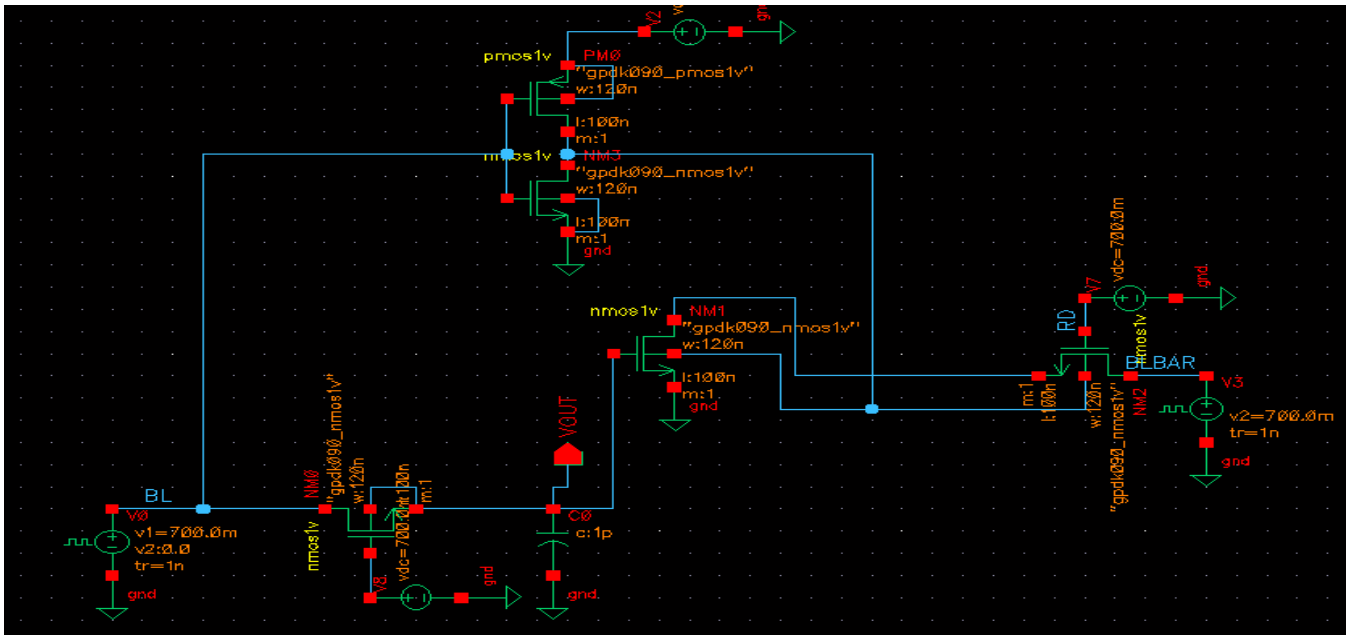

Fig. 6 Three Transistor DRAM with anti-body bias technique Implementation

3.4. Simulation Results of Three Transistor DRAM Cell

The transient response and leakage current waveform are shown in the figure below for the traditional cmos technique, double gate finfet technique and Anti-body bias techniques with parametric variation i.e variation in supply voltage and the capacitance value.

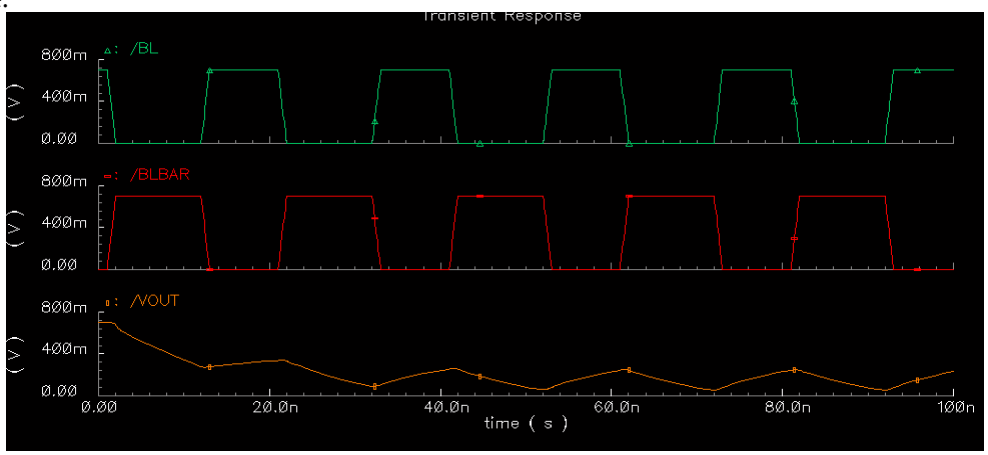

Fig. 7 Basic three Transistor DRAM Transient responses

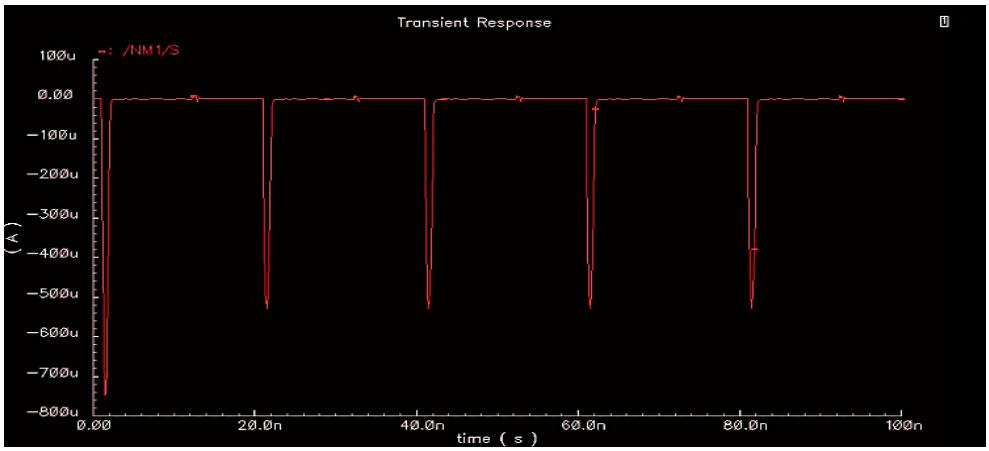

Fig. 8 Basic three Transistor DRAM leakage current

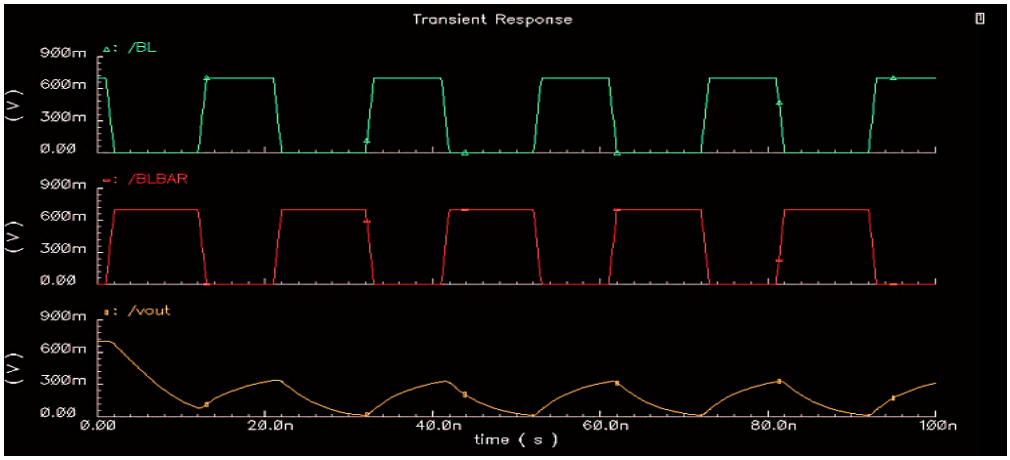

Fig. 9 Three-transistor DRAM with DG-Finfet technique transient response

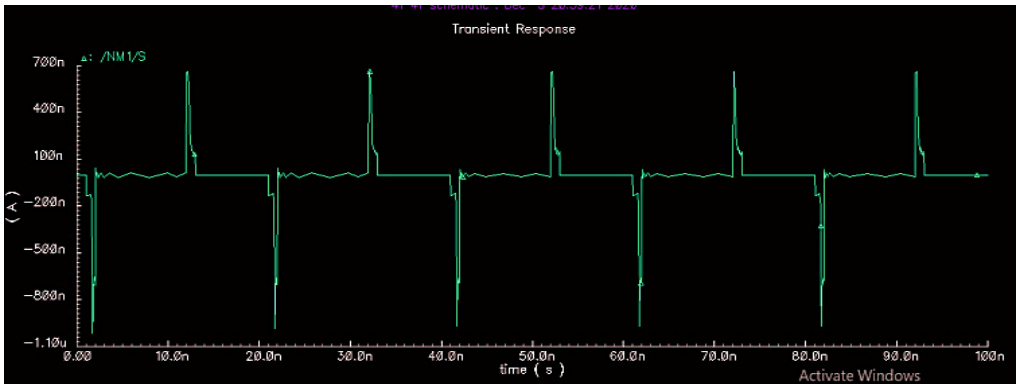

Fig. 10 Three-transistor DRAM with DG-Finfet technique leakage current

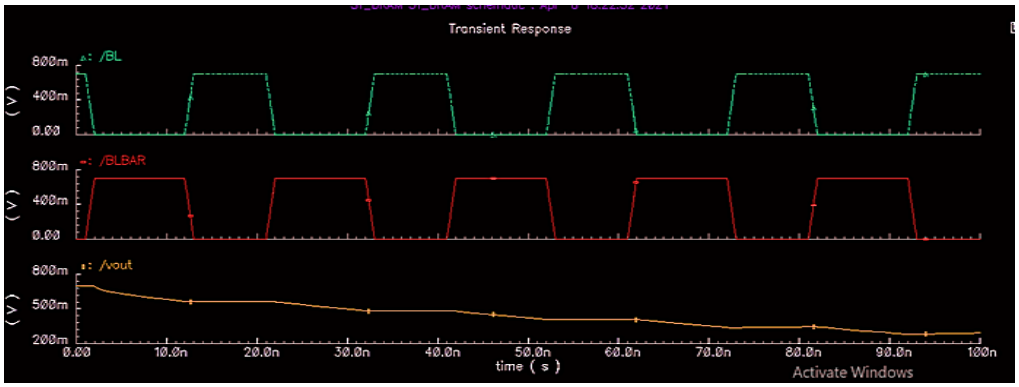

Fig. 11 Three-transistor DRAM with anti-body bias technique transient response

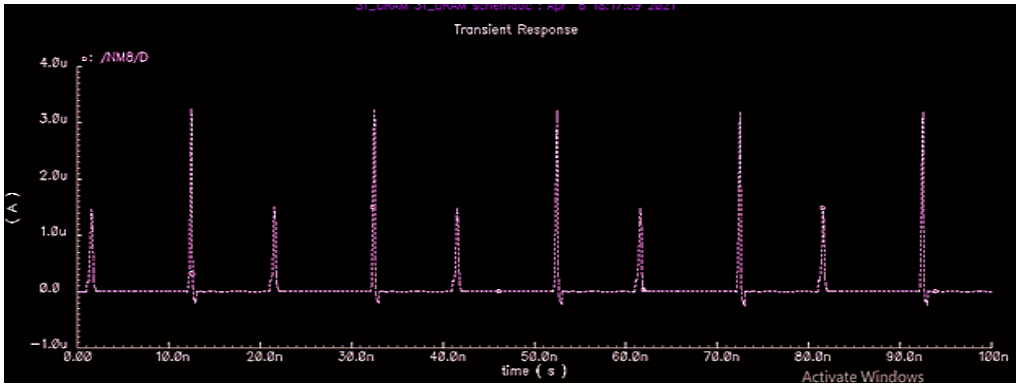

Fig. 12 Three-transistor DRAM with anti-body bias technique leakage current

4. Results and discussion

The proposed work is carried out for optimization of performance improvement parameters in high-density dynamic random access memories in real-time data storing applications. The 3T DRAM is implemented and simulated with various leakage reduction techniques i.e cmos, double gate finfet and anti-body bias technology. By parametric variation leakage parameters are calculated and comparative analysis has been carried out for cmos, double gate finfet and anti-body bias technology. The simulation results of cmos technology, double gate finfet technology and anti-body bias technology are shown in Table 1, Table 2, Table 3, Table 4, Table 5 and Table 6 respectively.

By parametric variation i.e. supply voltage and capacitance values variation, the Leakage current was observed maximum in the cmos technique, moderate in the double gate finfet technique and minimum in the anti-body bias technique. In supply voltage variation leakage current reduction is observed at 75% in the finfet technique and 82% observed in the anti-body bias technique. In capacitance value variation leakage current reduction is observed at 94% in the finfet technique and 96% observed in the anti-body bias technique.

The comparative analysis of the implementation of 3T DRAM is shown with the cmos technique, Finfet technique and Anti-Body bias technique by using a parametric variation. By variation in supply voltage and capacitor values, the leakage parameter variations are shown in the above table.

Table 1. Leakage Current Results

Case A: Variation in supply voltage [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Capacitor=1pF, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body BiasTechnique**
Sr. No.	**Variation in Supply Voltage(V)**	**Cmos_Leakage_Current (uA)**	**Finfet_Leakage_Current (uA)**	**Anti Body Bias_Leakage_ Current(uA)**
1	0.5	1.3	0.1	0.01
2	0.7	2.2	0.2	0.1
3	1	2.7	0.6	0.44
4	1.2	3.6	0.78	0.56
5	1.5	5	1.23	0.89
Case B: Variations in Capacitance value [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Constant Supply Voltage=0.7V, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body BiasTechnique**
Sr. No.	**Variation in Capacitor Value (pF)**	**Cmos_Leakage_Current (uA)**	**Finfet_Leakage_Current (uA)**	**Anti Body Bias_Leakage_ Current(uA)**
1	1	2.2	0.2	0.01
2	2	1.8	0.08	0.05
3	3	1.6	0.06	0.45
4	4	1.2	0.044	0.033
5	5	0.6	0.032	0.022

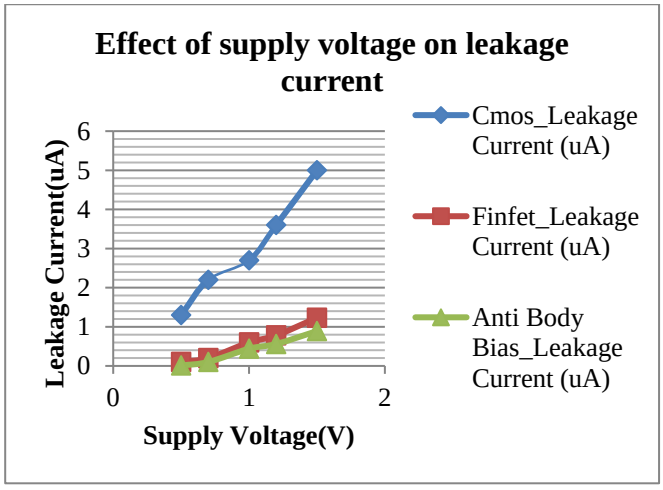

Fig. 13 Effect of supply voltage on leakage current

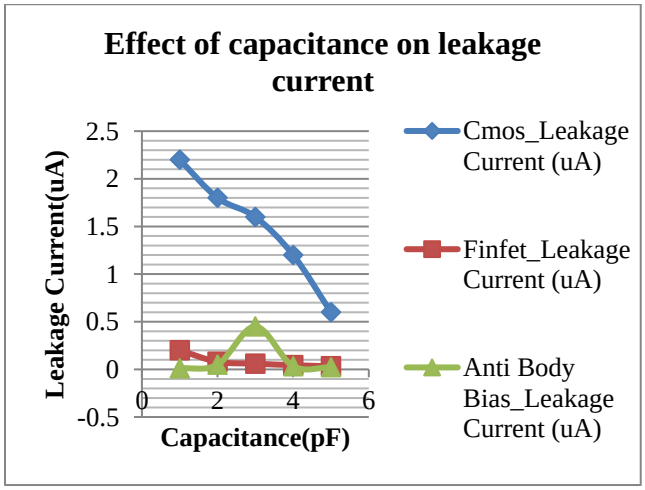

Fig. 14 Effect of capacitance on leakage current

By parametric variation i.e. supply voltage and capacitance values variation, Leakage power was observed maximum in the cmos technique, moderate in the double gate finfet technique and minimum in the anti-body bias technique. In supply voltage variation leakage power reduction is observed at 86% in the finfet technique and 88% observed in the anti-body bias technique. In capacitance value variation leakage power reduction is observed at 97% in the finfet technique and 98% observed in the anti-body bias technique

Table 2. Leakage Power Results

Case A: Variation in supply voltage [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Capacitor=1pF, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body BiasTechnique**
Sr. No.	**Variation in Supply Voltage(V)**	**Cmos_Leakage_Power (uW)**	**Finfet_Leakage_Power (uW)**	**Anti Body Bias_Leakage_ Power (uW)**
1	0.5	6.8	0.08	0.05
2	0.7	6.1	0.1	0.01
3	1	2.7	0.6	0.5
4	1.2	4.3	0.7	0.6
5	1.5	7.5	0.98	0.88
Case B: Variations in Capacitance value [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Constant Supply Voltage=0.7V, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body BiasTechnique**
Sr. No.	**Variation in Capacitor Value (pF)**	**Cmos_Leakage_Power (uW)**	**Finfet_Leakage_Power (uW)**	**Anti Body Bias_Leakage_ Power (uW)**
1	1	6.1	0.1	0.01
2	2	1.2	0.076	0.066
3	3	1.18	0.054	0.044
4	4	0.9	0.036	0.022
5	5	0.8	0.022	0.01

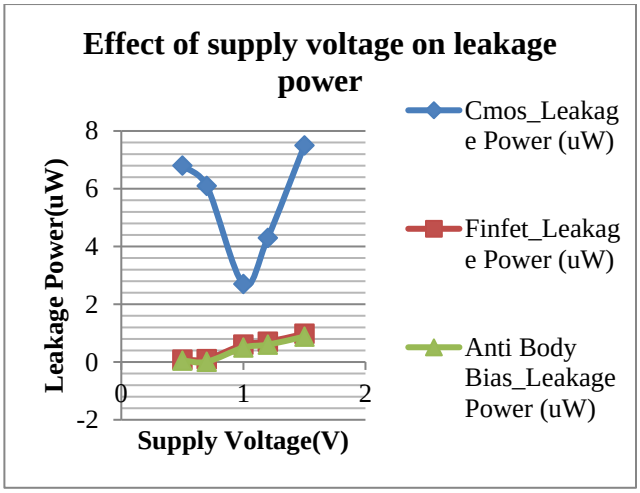

Fig. 15 Effect of supply voltage on leakage power

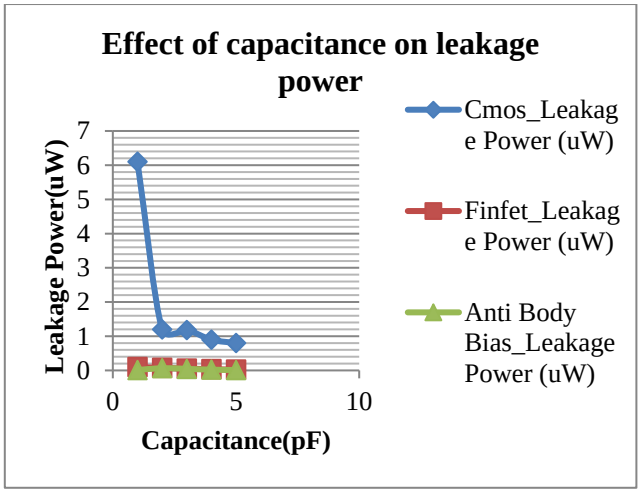

Fig. 16 Effect of capacitance on leakage power

By parametric variation i.e. supply voltage and capacitance values variation, the Average current observed is maximum in the cmos technique, moderate in the double gate finfet technique and minimum in the anti-body bias technique. In supply voltage variation average current reduction is observed at 38% in the finfet technique and 42% observed in the anti-body bias technique. In capacitance value variation average current reduction is observed at 53% in the finfet technique and 55% observed in the anti-body bias technique.

Table 3. Average Current Results

Case A: Variation in supply voltage [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Capacitor=1pF, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body BiasTechnique**
Sr. No.	**Variation in Supply Voltage(V)**	**Cmos_Average_Current (uA)**	**Finfet_Average_Current (uA)**	**Anti Body Bias_Average_ Current (uA)**
1	0.5	9.9	5.4	5.2
2	0.7	11.6	6.6	6.3
3	1	15.8	8.9	8.2
4	1.2	16.5	10.1	9.8
5	1.5	17.6	10.8	10.1
Case B: Variations in Capacitance value [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Constant Supply Voltage=0.7V, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body BiasTechnique**
Sr. No.	**Variation in Capacitor Value (pF)**	**Cmos_Average_Current (uA)**	**Finfet_Average_Current (uA)**	**Anti Body Bias_Average_ Current (uA)**
1	1	11.6	6.6	6.1
2	2	11.01	6.2	5.9
3	3	11.04	5.8	5.3
4	4	11.08	5.4	5.1
5	5	11.03	5.1	4.9

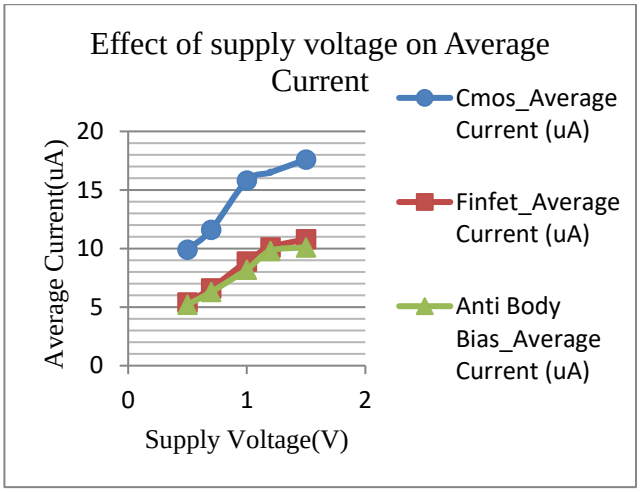

Fig. 17 Effect of supply voltage on average current

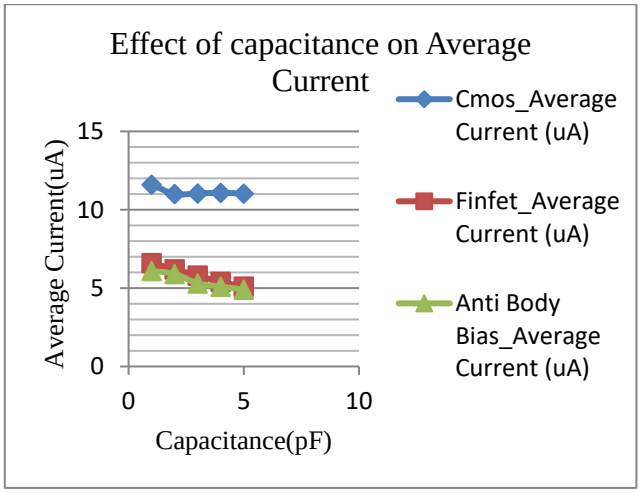

Fig. 18 Effect of capacitance on average current

By parametric variation i.e. supply voltage and capacitance values variation, Average power was observed as maximum in the cmos technique, moderate in the double gate finfet technique and minimum in the anti-body bias technique. In supply voltage variation average power reduction is observed at 38% in the finfet technique and 40% observed in the anti-body bias technique. In capacitance value variation average power reduction is observed at 53% in finfet technology and 59% observed in the anti-body bias technique.

Table 4. Average Power Results

Case A: Variation in supply voltage [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Capacitor=1pF, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body BiasTechnique**
Sr. No.	**Variation in Supply Voltage(V)**	**Cmos_Average_Power (uW)**	**Finfet_Average_Power (uW)**	**Anti Body Bias_Average_ Power(uW)**
1	0.5	4.95	2.7	2.2
2	0.7	8.12	4.62	4.33
3	1	15.8	8.9	8.2
4	1.2	19.8	12.12	11.8
5	1.5	26.4	16.2	15.8
Case B: Variations in Capacitance value [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Constant Supply Voltage=0.7V, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body BiasTechnique**
Sr. No.	**Variation in Supply Voltage(V)**	**Cmos_Average_Power (uW)**	**Finfet_Average_Power (uW)**	**Anti Body Bias_Average_ Power(uW)**
1	1	8.12	4.62	4.2
2	2	7.707	4.34	3.99
3	3	7.728	4.06	3.67
4	4	7.756	3.78	3.21
5	5	7.721	3.57	3.11

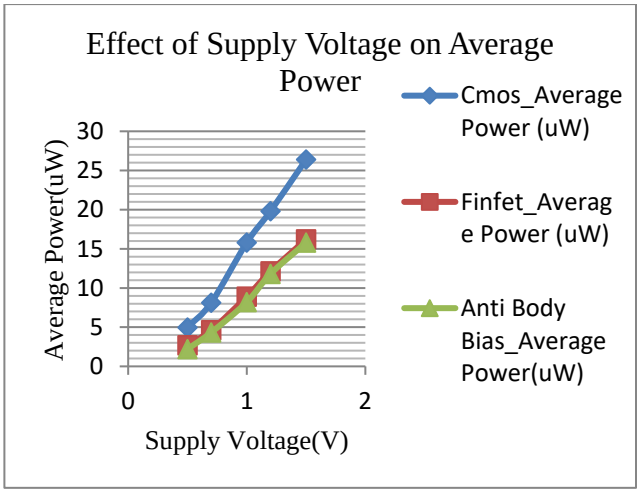

Fig. 19 Effect of supply voltage on average power

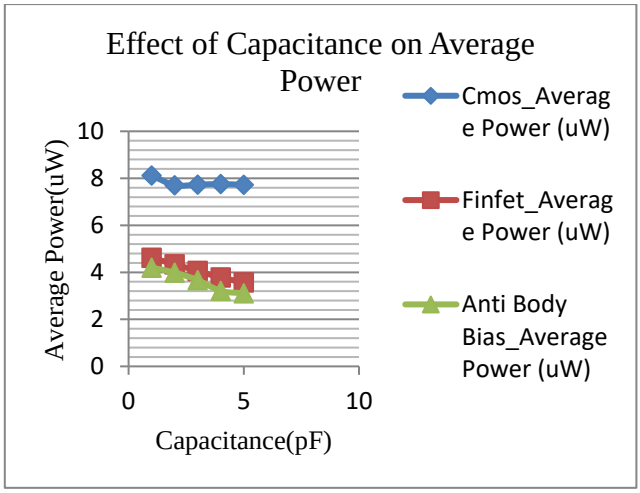

Fig. 20 Effect of capacitance on average power

By parametric variation i.e. supply voltage and capacitance values variation, Retention time was observed as a minimum in the cmos technique, moderate in the double gate finfet technique and maximum in the anti-body bias technique. In supply voltage variation retention time improvement is observed at 0.3 us in the cmos technique, 1.219 us in the finfet technique and 1.68 us in the anti-body bias technique. In capacitance values, variation retention time improvement is observed at 5.833 us in the cmos technique, 109.375 us in the finfet technique and 159.09 us in the anti-body bias technique. By using substrate biasing and an inverter circuit in the anti-body bias technique the retention time improvement is observed.

Table 5. Retention Time Results

Case A: Variation in supply voltage [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Capacitor=1pF, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body Bias Technique**
Sr. No.	**Variation in Supply Voltage(V)**	**Cmos_Retention_Time(Th) (us)**	**Finfet_Retention_ Time(Th) (us)**	**Anti Body Bias_Retention_Time(Th) (us)**
1	0.5	0.384	5	50
2	0.7	0.318	3.5	7
3	1	0.37	1.666	2.27
4	1.2	0.333	1.538	2.14
5	1.5	0.3	1.219	1.68
Case B: Variations in Capacitance value [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Constant Supply Voltage=0.7V, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body Bias Technique**
Sr. No.	**Variation in Supply Voltage(V)**	**Cmos_Retention_Time(Th) (us)**	**Finfet_Retention_ Time(Th) (us)**	**Anti Body Bias_Retention_Time(Th) (us)**
1	1	0.318	3.5	70
2	2	0.777	17.5	28
3	3	1.312	35	4.66
4	4	2.333	63.636	84.84
5	5	5.833	109.375	159.09

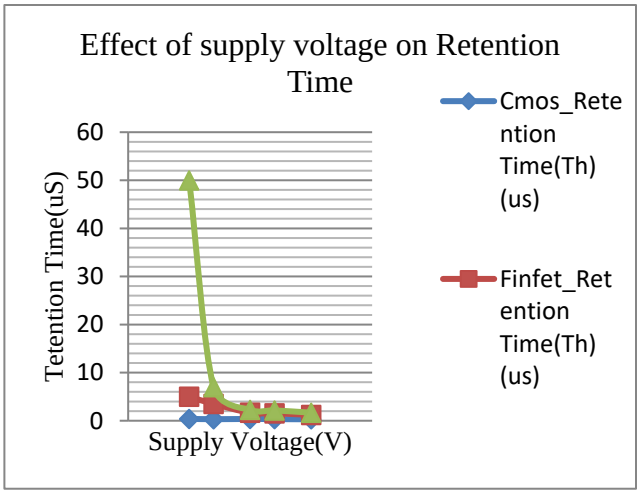

Fig. 21 Effect of supply voltage on Retention time

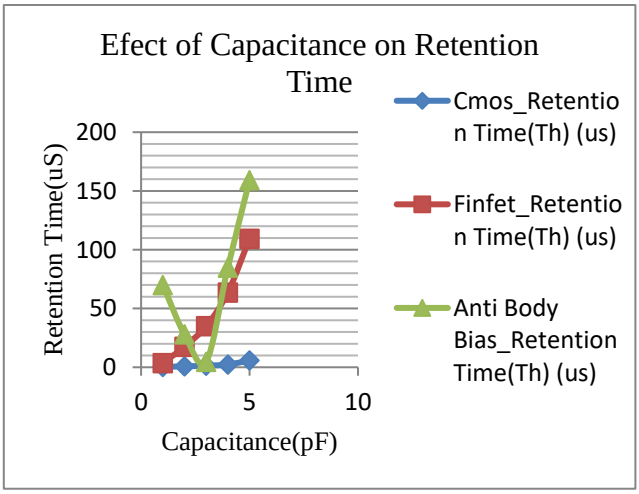

Fig. 22 Effect of capacitance on retention time

By parametric variation i.e. supply voltage and capacitance values variation, Refresh frequency was observed as maximum in the cmos technique, moderate in the double gate finfet technique and minimum in the anti-body bias technique. In supply voltage variation refresh frequency reduction is observed at 1660 khz in the cmos technique, 410 khz in the finfet technique and 297.61khz in the anti-body bias technique. In capacitance values, variation refresh frequency reduction is observed at 85.71 khz in the cmos technique, 4.57 khz in the finfet technique and 3.142 kHz in the anti-body bias technique.

Table 6. Refresh Frequency Results

Case A: Variation in supply voltage [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Capacitor=1pF, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body Bias Technique**
Sr. No.	**Variation in Supply Voltage(V)**	**Cmos_Refresh_Frequency (Frefresh) (Khz)**	**Finfet_Refresh_Frequency (Frefresh) (Khz)**	**Anti Body Bias_Refresh_Frequency (Frefresh) (Khz)**
1	0.5	1300	100	10
2	0.7	1570	142.85	71.42
3	1	1350	300	220.26
4	1.2	1500	325	233.644
5	1.5	1660	410	297.619
Case B: Variations in Capacitance value [Transistor Width(W)=120nm, Transistor Length(L)=100nm, Constant Supply Voltage=0.7V, Technology=90nm]				
Techniques		**CMOS Technique**	**FINFET Technique**	**Anti Body BiasTechnique**
Sr. No.	**Variation in Supply Voltage(V)**	**Cmos_Refresh_Frequency (Frefresh) (Khz)**	**Finfet_Refresh_Frequency (Frefresh) (Khz)**	**Anti Body Bias_Refresh_Frequency (Frefresh) (Khz)**
1	1	1570	142.85	7.142
2	2	642.86	28.57	17.857
3	3	380.95	14.28	107.296
4	4	214.28	7.85	5.893
5	5	85.71	4.57	3.142

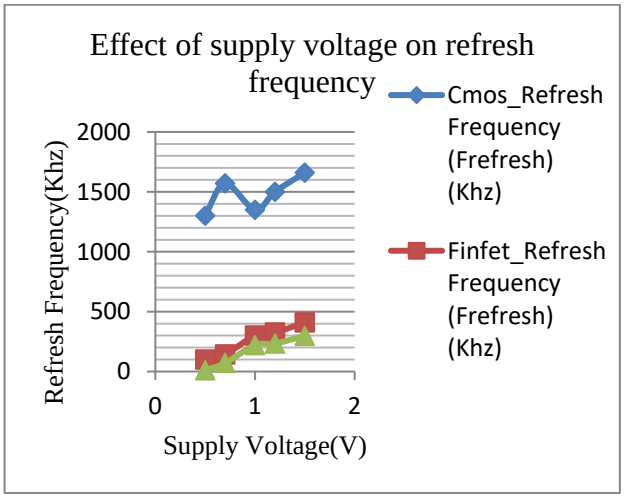

Fig. 23 Effect of supply voltage on refresh frequency

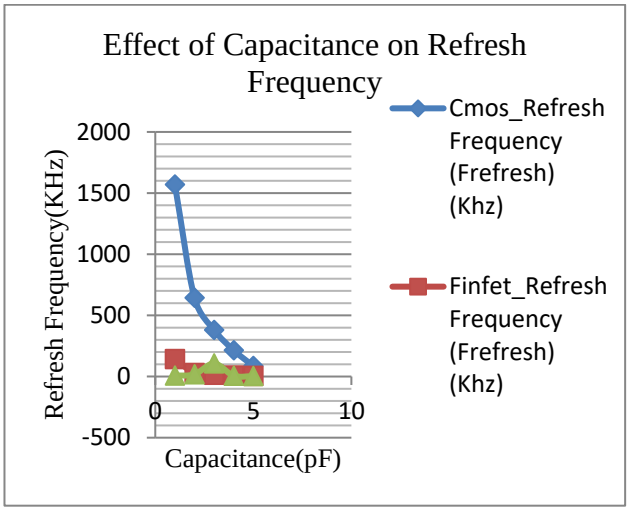

Fig. 24 Effect of capacitance on refresh frequency

5. Conclusion

Evolution in VLSI technology offers to scale parameters useful for the reduction in device size, small geometrical area, low operating voltage, minimum current capability and optimized storage capacity in semiconductor memories. The comparative analysis of 3T DRAM is carried out with cmos, finfet and anti-body bias leakage reduction techniques using a parametric variation. It has been observed that the leakage parameters reduce great extent in the anti-body bias technique as compared to the finfet and cmos technique similarly retention time improvement is observed in the anti-body bias technique as compared to cmos and finfet techniques. Retention time enhancement is observed and correspondingly refresh frequency goes down and it does not affect the dynamic random access memory performance. Also, improvement in retention time parameters prevents the loss of information in semiconductor memories.

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